Meeting minutes for team meeting-3

Date: February 26th, 2019

Location: Power lab (GJL 102)

Time: 2:30PM - 3:30 PM

Attendees: Dr. Herbert Hess, Zhengqi Li, Xin Han.

Note Taker: Manasa Pothamsetty

Q1: How many poles for the DFIG that is being used?

Ans: Data plate provides the rpm and frequency which can be used to calculate the number of poles. for this DFIG it should be approximately 5.

Number of poles = 120*f/rpm

Q2: how to determine frequency of PWM.

Ans: There will be 2 frequencies one is an underlying frequency of 60Hz and the other is determined depending on what voltage we need at the capacitor.

Q3: What will be a good goal for the end of this semester?

Ans: Modeling the DFIG and getting a DC voltage on the Capacitor will be a good goal.

- Open Circuit and short circuit test (OTC and STC are performed to find the parameters that will be used to model the DFIG):
 - o If slip=0 open circuit test
 - If slip =1 short circuit test (I.e. Zero speed at the rotor).
- We can either make 2 or 1 model for super synchronous and sub synchronous modes depending on our convenience and understanding.
- Verify the parameters such as Torque and speed.

Challenge: variable frequency might result in small voltage across the Capacitor.

Note: Next meeting will be held on Thursday (March 7th, 2019) at 12:30 PM in Power lab instead of Tuesday (March 5th) due to snapshot.