Senior Design Schedule

Project: FPGA Data Aquisition And Control

	Last	Updated:	10/8	8/19																																		
		Year					2019										2020																					
		Month		Se	ot	Oct				Nov					Dec			Jan			Feb				Mar			Apr				May						
Task Description	Duration	Assigned	9/2	9/9	9/16 9/23	3 9/30	10/7	10/14	10/21 1	10/28	11/4 11	1/11 11	l/18 11,	/25 12	2/2 12/9	12/16 1	2/23 1	2/30 1	/6 1/13	3 1/20	1/27	2/3	2/10	2/17	2/24	3/2	3/9	3/16	3/23	3/30	4/6	4/13	4/20	4/27	5/4	5/11	5/18	5/25
Literature Review	4 Weeks	All																																				
Subject Matter Expert Interviews	3 Weeks	All																																				
Design Validation Plan	2 Weeks																																					
Project Value Proposition	2 Weeks																																				1	
Control Loop Design	3 Weeks																																					
Control Loop Testing	1 Week																																					
Interferometer Design	8 Weeks																																				1	
Build/Debug Interferometer Prototype	3 Weeks																																					
Test Interferometer Prototype	2 Weeks																																					
Write Report Outline	2 Weeks																																				1	
Write Technical Report	3 Weeks																																					
Order Red Pitaya Boards + Lead time	1 Week	Jared																																			1	
Design Board Combination Bus	3 Weeks																																					
Prototype Board Combination Bus	1 Week																																					
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Length of Critical Path:	24 Weeks	I													I						1 1				I								I I		I	l	I	_

Length of Critical Path:

Slack Time:

2 Weeks