

Senior Capstone Design

Project: [Hardware in the Loop Design](#)

Primary Author: [David Lowe](#)

Team: [Simulation Sages](#)

Date: **3/2/2021**

Design Validation Plan & Results (DVP&R)

Requirement	Test	Test Subject	Target Date	Result	Recommendation
Compiled RSCAD model of IEEE 13 bus power System with 3 PV Inverters Connected.	Model runs on RTDS	Power System RSCAD model	3/9/21		
Controlled power output for each PV inverter.	Run model on RTDS and adjust power output controls in real time and verify the power readings are changing for specific busses.	Power System RSCAD model	3/16/21		
PV inverter control through SEL RTAC	Run Model on RTDS and adjust PV inverter inputs. Verify the RTAC adjusts PV controls as planned.	Power System RSCAD model and SEL RTAC.	3/23/21		
Functional RTAC HMI	Run model on RTDS and use HMI to manually adjust PV inverter controls in real time.	Power System RSCAD model and SEL RTAC HMI.	3/30/21		
Lab procedure documentation is clear and usable for power students.	Invite a EE student to go through the procedure in the lab with the equipment and give feedback.	Lab procedure document	4/6/21		