

Into the Wind

Doubly-Fed Induction Generator Rotor Side Converter Design

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EXECUTIVE SUMMARY

This project focuses on the design and implementation of a rotor side converter (RSC) to monitor a doubly-fed induction generators (DFIG's) torque, current and voltage output in order to command an input waveform that will stabilize the DFIG with the grid at 60Hz. The design of the RSC needs to be modular so that further advancement with this design can be easily implemented as well as providing ease of component replacement if any damaging faults occur during research. Along with being modular the design was implemented to be robust, both in terms of physical strength to prevent any damage during relocation of the device and in terms of electrical parameters to ensure a long life span of components. To address these needs devices have been chosen with ratings having a safety factor up to 125%, isolation between low voltage and high voltage devices has been put in place, extra protection circuits were included in the design, a turn on procedure was developed to minimize transients, and devices were mounted in a manner allowing for easy dismantle and reassembly. Further implementations addressing the needs of this project include control code that is easily accessible, can be updated using free tools aiding in the configuration of the controller, offers plenty of optimizations to ensure high performance of the controller, and adds flexibility to the system. Completion of this project will aid in the advancement of wind energy systems by allowing further research to be conducted on subsynchronous resonance of a DFIG.

I. BACKGROUND

The DFIG is the core component of type III wind energy conversion systems. Due to a shifting societal priority towards renewable energy, these systems are becoming much more commonplace. With the rise of wind energy systems, there is an increasing need to ensure these systems are stable and fault tolerant, which drives the need for research into

how these systems interact with the grid and how

they can be made more tolerant to transients and unstable situations, such as subsynchronous resonance. In order to research these conditions and how to improve the stability of the DFIG in general, there is a need for a high performance, stable, robust, isolated test system that can be utilized in a lab under controlled conditions and be subjected to various tests. This will allow phenomena involving the DFIG and its interaction with power systems to be researched in a safe and efficient way.

II. PROBLEM DEFINITION

Completion of this project is defined by designing and implementing a three phase inverter and its protection components, writing and implementing code for space vector modulation and field oriented control, providing isolation between the low voltage and high voltage components, designing and implementing sensors to gather data needed to command the RSC, assembling the prototype, and testing the prototype to validate the functionality of the design. Deliverables following completion of this project include the RSC stand and test results justifying proper function of the device.

Regarding specifications of this project the design was to be completed in a manner that would produce a prototype that was modular, robust, utilized startup and fail safe procedures in coding, and incorporated adequate isolation. Constraints given for the project included the RSC being able to handle an input of up to 340V from a DC bus, stabilizing a generator at 60Hz that would be operating at frequencies between 0-60Hz when a RSC was not implemented, and being able to read sensor inputs and operate the 3-phase inverter at a minimum frequency of 20kHz.

III. PROJECT PLAN

The design of an RSC has three major focuses: software design and testing, hardware

design and testing, and manufacturing. Team Into the Wind consisted of Keegan Miley-Hunter the Chief PCB Designer and Manufacturer, Mason Taylor the Chief Programmer, and Mason Ulrich the Chief Power Electronics Expert and Budget Manager. Roles such as Meeting Leader, Documenter, and Recorder are shared amongst the team members in a series of rotations.

Step one of this project included a 4-5 week period devoted solely to researching DFIGs. Following the research period the plan was to start hardware selection and design verification (simulations). Original intention was to start design verification immediately after our allotted learning time was complete, however given the information acquired during the learning period our schedule was adjusted to start hardware selection on February 16th. Once the process of selecting devices was underway the design verification procedures began. The previously mentioned topics provided us with a complete schedule for the first semester of this project and were continued over the summer alongside hardware module tests.

The remainder of our project plan involved the continuation of subsystem testings over the course of the second semester as well as finalizing the project code, and manufacturing and mounting the devices onto the RSC stand. To see a more detailed representation of our project outline including specific dates and those responsible for each task view appendix A. In appendix A you will find two versions of our Gantt chart. The first version of the Gantt chart displays the broad topics of the project outline while the second includes all of the tasks related to each of the main categories.

IV. CONCEPT EVALUATION

A. *Space Vector Modulation*

Evaluation of the Space Vector Modulation (SVM) algorithm began with studying and understanding the basic concept during the learning phase. Utilizing some basic simulations, the specific equations for our implementation of SVM were collected and used to create a more detailed simulation that accurately tested the

implementation of SVM that will be used for the physical test bench. Essentially, this test consists of utilizing SVM in current control mode, determining the PWM scheme to use, devising an algorithm for causing the fewest switching events possible, and finally testing how this interacts with an inductive load.

To test active current control, a PI controller was implemented in the simulation. The three phase current measured in the load was converted to Direct-Quadrature (dq) axis rotating reference frame in order to have stable value (i.e. current values are essentially constants), then it is not difficult to implement a PI controller that can maintain the currents very close to the command, even as the command changes. Next, we decided to use center aligned PWM with three channels (one for each phase leg) with six outputs (three positive and three negative or complementary). This makes applying the derived vector straightforward and provides protection for power electronics by maintaining the switch configuration in one of the eight possible safe states. Using center aligned PWM also naturally allows us to reduce the number of switching events (by ensuring that all states are not toggled to on/off at the beginning of each cycle) while also staying in each state for the correct amount of time. In each cycle, the SVM algorithm generates a time for each of three states. These consist of two adjacent non zero states and a zero state (the remaining time for a cycle). There are two zero states where there is no net current flow through the balanced three phase load (i.e. states 000 and 111). By properly utilizing these zero states, we are able to ensure that only one phase leg changes state at a time. See Appendix J for details on the implementation and calculations.

With the PWM waveform generated, the simulation tests how this waveform would interact with an inductive load. To test this, we generate a transfer function for each phase of the load. We feed the voltage waveform generated by PWM through the transfer function in order to obtain a current estimate. This is done in each phase and is used to calculate the overall current in the dq rotating reference. This overall current is compared to the command to

generate an error function which is used by the PI controller to actively adjust the command to control the current phase and magnitude.

B. Power Electronics

Power electronics evaluation began by familiarizing ourselves with the interactions between the devices we would be using. To do so the first step was to investigate the integration of the gate driver with the IGBTs. In our research we came up with two possible solutions for our design: the first solution was to implement a three-phase gate driver with a six pack IGBT module and the second solution was to design the RSC using a three-phase gate driver with three two pack IGBT modules. Each solution also incorporated the use of a high-side and low-side gate driver as a means of initial research to avoid damaging our three-phase gate driver during the learning phase. While both methods are feasible due to the lack of equipment on hand to mount the six pack IGBT module the final design was chosen to utilize three two pack IGBT modules. The finalized choice for devices were the 6EDL04I06PT by Infineon as the three-phase gate driver, the IR2101(S) by Infineon as the high-side and low-side (single phase) gate driver, and the FF200R06KE3 by Infineon for the two pack IGBT module. Main features of the three-phase gate driver that dictated our choice was the devices voltage rating of 620V, the ability for separate control of each driver, and the devices extra built-in protection to detect over current, under voltage supply and signal interlocking capability of every phase. The choice of the IR2101 stemmed from our decision of the three-phase gate driver we chose. Since it would be serving as a research tool to familiarize ourselves with the gate driver and IGBT interactions of our design, the IR2101 was chosen due to its similarities to Infineon's 6EDL04I06PT gate driver. As for the IGBT module choice, the main parameters of the FF200R06KE3 that led to our choice was its 600V collector-emitter voltage, its low collector-emitter saturation voltage of 1.6V, its 200A continuous collector current, and the

devices small delay/rise times for both turn on and turn off that corresponded to a dead time of approximately 1us.

After having specced out gate drivers and IGBTs, models for each device were able to be plugged into LTSpice (Spice) simulations to verify the design. Spice simulations were initially constructed for a simple single leg design to observe component integration and were later adapted to an H-bridge design. The H-bridge simulation was completed to investigate component integration and the turn on/off delays of each IGBT to ensure the dead time needed between the turn on/off of each leg of IGBTs to avoid faults caused by short circuiting the system. In Appendix B you will find schematics for both the single leg simulation and H-bridge simulation. Results of the single leg simulation are not included since a more advanced single leg simulation will be discussed that includes the protection circuits integrated into our design. All Spice files can also be found in our portfolio.

Following verification of the integration of the gate driver and IGBTs the next power electronics design revolved around incorporating the protection circuits and components. Protection for our design focused on two main topics: snubbers and MOVs. Snubber circuits were chosen in order to minimize the switching losses of our design while also protecting the IGBTs by minimizing the losses of each IGBT and therefore reducing heat transfer in the devices making the design more robust. The first step in designing the snubber circuit required calculations to be made, these calculations can be seen in detail in Appendix C. From the calculations and the use of the principle of duality to determine component values needed for the turn off and turn on snubbers the components were integrated into the original single leg Spice simulation to verify functionality. During this process many reiterations were conducted after slight changes in inductor, capacitor and resistor values of the snubber circuits in order to manipulate the voltage and current waveforms of the IGBT in a manner that produced an acceptable power loss in the device. Alterations of these components were also made in order to produce voltage and

current values through the IGBT below the device ratings. The results of the finalized circuit along with the schematic for the simulations can be found in Appendix C. In the results you will see that the finalized values for each component of the snubber circuits are as follows: 50 Ohm resistors, 1.2uH inductors, .12uF capacitors. Another observation to be noted concerns the turn on snubber. In the results for the turn on snubber you will notice the power results appear to be very large, however device ratings are concerned with average power and not instantaneous power. Performing calculations led to an average power of just 38W due to the short interval of time in which the 4kW were being produced (see Appendix C for details).

Alongside snubbers the other means of protection mentioned were the use of MOVs. MOVs were utilized as an extra layer of protection for the IGBTs in order to act as a path for current to flow if an unexpected spike were to occur. Due to this the MOV was selected based on its varistor voltage that falls in the range of 420-520V, its continuous rms voltage of 300V, and its peak pulse current of 100A for an 8/20us current waveform.

The last two design components to be simulated for verification and understanding purposes were the three-phase inverter and the high voltage (HV) side power supply. To complete the three-phase inverter simulation an ideal circuit had to be implemented in order for Spice to run in a timely manner due to the complexity of timing involved with the fully integrated design of the three-phase inverter. A schematic for the ideal three-phase inverter can be found in Appendix D along with its results. From the schematic you can observe that the ideal three-phase inverter did not include the chosen components, instead it utilized ideal sources and switches. Due to this fact this simulation served as a means of understanding and having a visual representation of the end goal of this project and reference for tests in the lab.

Concluding the power electronics verification stage was a simulation to validate component selection for the HV power supply which consisted of a 120:12V transformer, a full

wave rectifier, smoothing capacitors, and two DC-DC converters for supplying power to the receivers and transmitter on the HV side and the fault pin of the gate driver. To view the schematic and results for the Spice simulation regarding the HV power supply see Appendix E. In Appendix E you will see the schematic which utilizes a voltage source to represent the voltage seen from the output of the 120:12V transformer and a current source depicting the total load current being drawn by the receivers/transmitter, DC-DC converters and the gate drive. While the DC-DC converters are needed to supply power to the receivers/transmitter and fault pin of the gate driver, the gate driver is able to be powered directly from the output of the full wave rectifier. This can be accomplished since the rectifier is producing a voltage just under 16V which meets the gate driver supply voltage range of 13-17.5V.

V. IMPLEMENTATION AND TESTING

A. Power Electronics Testings

With component specifications defined and verified through simulation the next step was to validate the choices made through hardware testing. The plan for hardware testing was to start with single components and integrate components following the verification that each component previously tested was working properly. This began by testing the optic links (transmitters, receivers, and fiber optics), testing the gate driver, integrating these components to be tested together by testing the microcontroller, optic links, gate driver, and IGBT modules on a small scale in a single circuit, and finally testing the air core inductor created for the turn on snubber. Along with these tests another test was conducted to observe that the HV power supply circuit was able to meet specifications and matched the results from simulations.

To conduct the first test all that was needed was our microcontroller and two breadboards to observe functionality of the microcontroller and the optic links and compare the signal delay created from the optic links in a test environment to the delay listed for the

devices in the datasheet. Test setups can be viewed in Appendix H. This test was also conducted on the perfboards created for each optic link to verify timing and ensure components were properly configured and soldered onto the perfboards. Results for these tests can also be found in Appendix H.

After testing optic links we moved onto testing the high-side low-side gate driver. This was first performed in complete isolation using power supplies to command input signals of the gate driver and observe the output ports. Once configurations of the gate driver had been reassured by test results, the gate driver was tested along with the IGBT module by creating a RC charge circuit consisting of the gate driver, the IGBT module, a RC load, a waveform generator to command the inputs of the gate driver, and a 6V source used to charge the circuit. A schematic for this setup and actual circuit build can be seen in Appendix H. Results for these tests will be found in our portfolio (these results are in the format of a video showing the charge and discharge of the capacitor). In the test the waveform generator was first utilized to create the input signals but later on the microcontroller was used to send the signals through our optic links. In both tests two square waveforms (inverse of each other) with a frequency of 22 Hz were sent as input signals allowing for full charge and discharge of the circuit.

Since we ended up making air core inductors to be used in the snubber circuits, tests to verify the inductance needed to be performed. Calculations were conducted to provide a starting point for inductor size, however after following test procedures the calculations were deemed inaccurate. Test procedures to measure the actual inductance were executed by creating a RL circuit, keeping the input voltage and frequency constant, measuring the voltage across the resistor, and altering the design of the inductor until the resistor voltage was half of the input voltage. This method works when maintaining a constant voltage and frequency based on the following formula to calculate inductance for this circuit:

$$\text{WHEN } V_R/V_{IN} = 1/2 \\ L = R \cdot \sqrt{3} / (2 \cdot \pi \cdot f)$$

The last test performed aimed to verify the integration of the HV power supply with the RSC design. This test first observed the input voltage the transformer saw from the wall outlet and what voltage level it was stepping the input down to. After observing these values the transformer output was connected to the rectifier circuit to observe the rectified voltage value. Since this test produced results that contradicted the values proposed by the transformer datasheet, the output from the full wave rectifier was not compatible with the input voltage range of the DC-DC converters selected. Therefore alterations to the circuit had to be performed to test the integration of the transformer, rectifier and DC-DC converter. To test the integration of these components a voltage divider was temporarily put in place using a 1.5kOhm and 4.7kOhm resistor to bring down the rectified voltage to 14.85V. With the rectified voltage now within the DC-DC converters rated voltage range of 9-18V the integration of the transformer, full wave rectifier and DC-DC converters was tested and the desired outputs of 3.3V and 5V from the DC-DC converters was verified. This test was performed only to validate the design layout for the HV power supply, by no means should a voltage divider be used in the final design.

B. Software Testings

With the SVM and PWM schemes implemented and tested in the simulation, we moved on to implementing and testing them on the microcontroller. Converting the simulation to C code to be run on the microcontroller was fairly straightforward, although some optimizations may be required if the final control loop is found to be running too slowly. For testing the SVM and PWM however, the algorithm ran plenty fast. The basic test algorithm runs a loop in which each iteration takes the command current and the dq reference frame angle and uses this information to run the SVM and generate the PWM switch times. These are then applied to the three

channels which are output on the motor control header pins on the microcontroller as 3.3V digital signals. To test that generated signals are correct, they were first inspected via an oscilloscope. After verifying to the extent possible with the oscilloscope, a circuit was constructed to better test the outputs. The circuit consisted of three Infineon IR2011 (single phase high/low side) gate drivers connected to the logic outputs of the microcontroller with the gate driver outputs driving the gates of six 60V NMOS power MOSFETs which stand in for the IGBTs that will be used in the final design. There are three high side MOSFETs and three for the low side, connected in the typical 3-phase inverter topology (see figure *Basic 3-Phase Inverter Topology* in Appendix D and Appendix H). Connected to the floating node on each leg of the inverter is the corresponding inductive load for that phase leg. In the case of the PWM small scale test performed for this project, both the simulation and the physical test used an R-L load consisting of a 100 Ohm resistor along with a 150 mH inductor. This provided a small and stable current at 60 Hz and allowed the current in each phase to be measured via the voltage across the resistor. One notable issue with the physical testing is that the microcontroller had to be physically modified to connect the PWM outputs to the motor control header pins (modifications required are bridging solder pads and removing components, these steps are listed in the microcontroller user manual). Another option is using the extension headers provided, as all signals are accessible from these headers, however the pin spacing is a non standard size and difficult to connect to with the standard jumpers. The next step for the small scale testing is to add in feedback via an ADC module to test closed loop current control. This was not finished as the onboard ADC modules would work but do not have accessible pins without board modifications or a custom breakout board/adaptor for the extension headers, and the external ADC module that was ordered to connect to the sensors on the power cart on have a custom PCB breakout board for the microcontroller extension headers. After this, the field oriented control algorithm can be

implemented and validated before integration testing with the higher voltage components.

VI. SYSTEM DESIGN

System design originated as a Spice schematic and evolved during the building phase of the project. A finalized Spice schematic can be seen in Appendix F displaying the general layout of components needed to complete this project. The schematic in Appendix F includes all equipment except for the sensors required to measure outputs from the wind turbine simulation machine.

In the schematic (working left to right) you will find a symbol depicting the microcontroller with input ports for readings it will be taking from the machine and the communication with the fault pin of the gate driver along with its output ports which include the power supply for the low voltage (LV) side, and the signal outputs to be communicated to the HV side through optic links to command the IGBTs. The next components you will find in this schematic are passive components to serve as noise filtration for the transmitters, the transmitters, a lead between the transmitters and receivers representing the fiber optic cables, and the receivers with their corresponding noise filtration components. Transmitters and receivers utilized for sending signals to control the IGBTs are located in the top portion while the two sets of optic links below are used for viewing the fault pin and commanding the enable pin of the gate driver. The aforementioned components make up the LV side of the RSC design as well as the link to the HV side.

From here the rest of the schematic found in Appendix F relates to the HV side of the RSC. The first configuration you will see located below the receivers and to the left of the gate driver is the HV power supply. As mentioned previously this consists of obtaining power from a wall outlet, stepping down the value utilizing a transformer, rectifying the voltage through the use of a full wave rectifier and smoothing capacitors and finally using DC-DC converters to supply power to the HV side

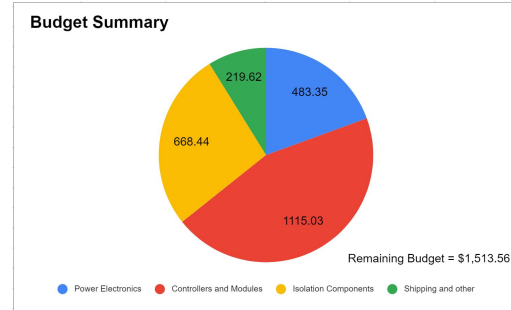
receivers/transmitter and gate driver fault pin. For simplification purposes the smoothing capacitors are lumped as one capacitor (to view actual component values used view Appendix E). The remaining portion of the design schematic consists of the gate driver, external components needed for the gate drivers function, the IGBTs and heatsink, the snubber components, and lastly the location of the DC rails (+/-).

Following the conceptual design layout of the RSC was the actual stand configuration and manufacturing process. The first step taken for integrating our design was to hand solder perfboards for each transmitter and receiver as well as a perfboard to house the full wave rectifier, smoothing capacitors and DC-DC converters. While completing the perfboards gerber files needed for the printing of the PCB which would consist of the gate driver and its external components were being completed. Once all perfboards were complete and gerbers were created for the gate driver PCB, stand assembly began. An image showing the current stand configuration can be seen in Appendix G. In this image you will see that all receivers/transmitter were mounted to the stand via mount rails that attach to the heatsink and are located at the top portion of the stand. The transmitters/receiver sending the signals to the ones viewed are directly across from the ones viewed on the LV side of the stand. Further investigation of this image shows the mounting of the HV power supply perfboard and the transformer (located below the receivers and mounted in the same manner as the receivers) along with the location for the gate driver PCB which is also mounted on the heatsink, but in front of the previously mentioned subsystems. The layout described allows for easy interconnection of each device. The last components viewable in the image of Appendix G are the IGBT modules, the snubber components and the negative rail with leads to the output ports of the RSC. Snubber components have been mounted directly to the negative rail and IGBT nodes to improve performance. This process was completed by

twist soldering the snubber components together.

VII. BUDGET SUMMARY

The total budget for this project was initially predicted to be \$3,600. Given our initial estimate we were given \$4,000 total to aid in the completion of the RSC design. By the end of the project we had spent \$1,115.03 on microcontrollers and modules, \$668.44 on isolation components, \$483.35 on power electronic components, and \$219.62 on shipping, our poster, and unused batteries. A breakdown of these costs along with the total remaining budget of \$1,513.56 can be seen in the pie chart below.



VIII. FUTURE WORK

Main steps involved with future work pertain to testing a fully integrated circuit since we were unable to prepare our prototype in time for testing. Before prototype testings are able to be completed a few minor steps also need to be performed. A general layout of these minor steps that will be discussed in more detail include pcb fabrication, HV side mounting, LV side stand configuration/mounting, and Field Oriented Control.

In regards to the PCB fabrication gerber files for the fabrication process have been created and can be found in the portfolio of this project. Alongside the gerber files that will be used for printing the PCB a few components that will be a part of the PCB still need to be specced out. The components that have not yet been chosen for the gate driver PCB involve the gate drivers built in protection. These

components are laid out in the final design schematic found in Appendix F, but the values of the components have not been specified.

Components still needing to be specced out include a capacitor that will be connected to the RCin port that will determine the reset time if a fault is to occur, a capacitor connected to the ITrip port that alters the threshold voltage of the pin, and a resistor connected to the ITrip pin (the need for this resistor is not clear). Getting the printing process of the PCB completed as soon as possible is highly recommended due to the troubles we had with the in house printing machine.

As for the mounting associated with the HV side of the stand the tasks listed below need to be completed:

- Mount PCB and make gate driver connections
- Twist solder snubber components (already in place)
- Drill extra holes on the heatsink for proper IGBT mounting
- Find the best placement for the positive rail and mount it
- Order new transformer
- Remove voltage divider from rectifier circuit
- Connect power supply outputs to optics and gate driver

To finish the minor tasks needing completion before prototype testing the last two items to address are the LV side stand configuration/mounting and the completion of the Field Oriented Control code. The optic link components are already in place, however a place designated for the microcontroller needs to be determined and connections to the optics and sensors will need to be made. To complete the final connections to all the sensors, we recommend a custom breakout board to connect to the extension headers of the microcontroller (CN5 & CN6 in the STM32G474 user manual) to organize the IO pins into a clean arrangement with standard spacing between pins (2.54mm spacing, which is equivalent to a typical breadboard). This would allow standard ribbon cables to be made to connect the digital IO of the microcontroller to the ADC module and the

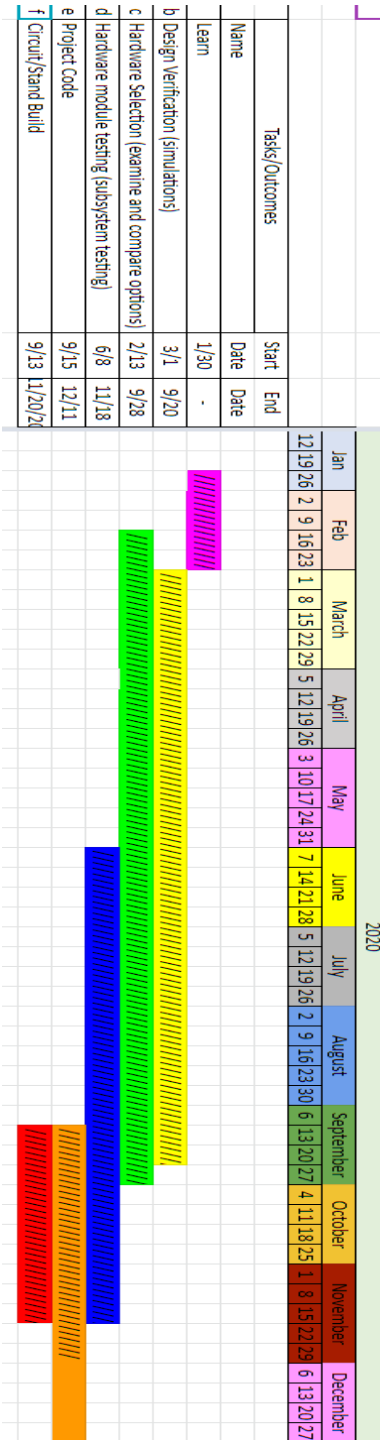
optics connected to the gate driver, as well as the digital connections to the encoder, and torque transducer from the wind turbine simulator. A schematic for this breakout board was created and includes the extension header connectors, all the individual ports, and a header for the PWM, encoder, and a power extension header. It was created with Altium CircuitStudio. It is recommended to finalize the schematic by adding dedicated headers for the torque transducer and anything else that a future team might find necessary, and have the PCB made as soon as possible. That will allow future tests and connections involving the microcontroller to go more smoothly. We have ordered the required components (namely, the Samtec headers to connect to the extension headers on the microcontroller and through hole pin headers) to make 4 of these breakout boards once the PCBs are made.

Once the breakout board is finished, and the field oriented control algorithm has been verified in small scale, the final system connection can be set up and all the components mounted to the power electronics cart. With a proper start up sequence, and instrumentation in place, the final integration testing will involve testing the gate drivers, IGBTs, and optics together, then testing these with a dummy R-L load (such as an inductor load bank and resistor load bank in series) along with the voltage and current transducers connected to the ADCs to ensure accurate readings. Once all these systems function properly, and closed loop current control is functioning as expected, the system can be tested with the wind turbine simulator and field oriented control. Passing this test should indicate that all components in the rotor side converter (RSC) are working correctly.

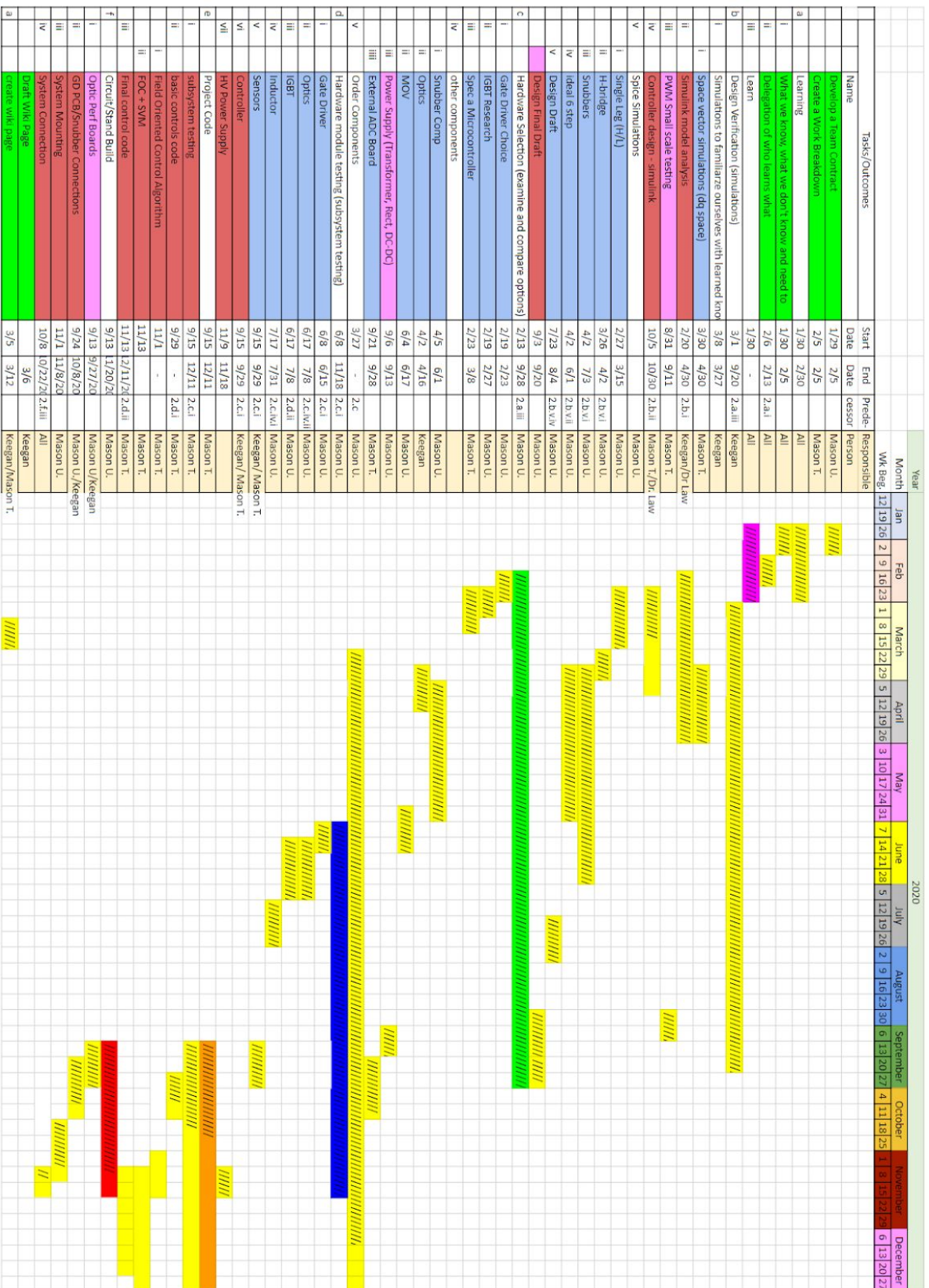
Since the majority of future tasks revolve around mounting/integrating components and performing tests on the completed prototype the remaining budget of \$1,513.56 should be sufficient for the next team.

Appendix

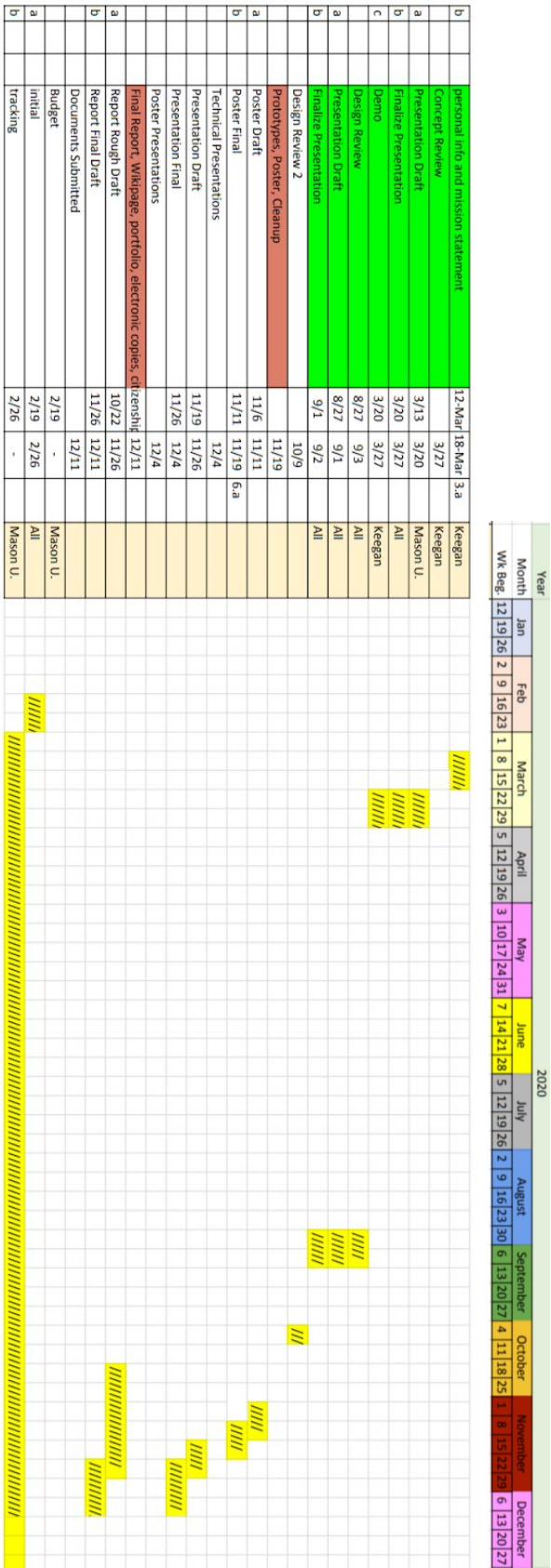
Appendix A (Gantt Chart)



Summarized Gantt Chart

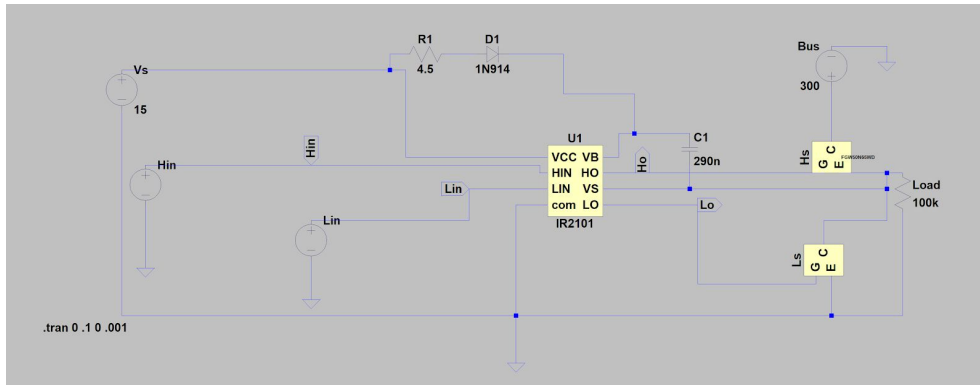


Full Gantt Chart Part 1

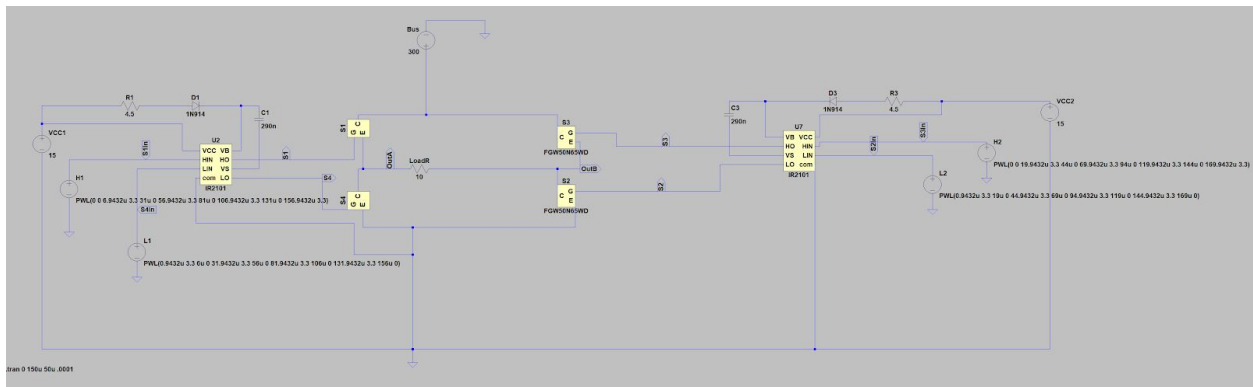


Full Gantt Chart Part 2

Appendix B (Single Leg & H-bridge Schematics)

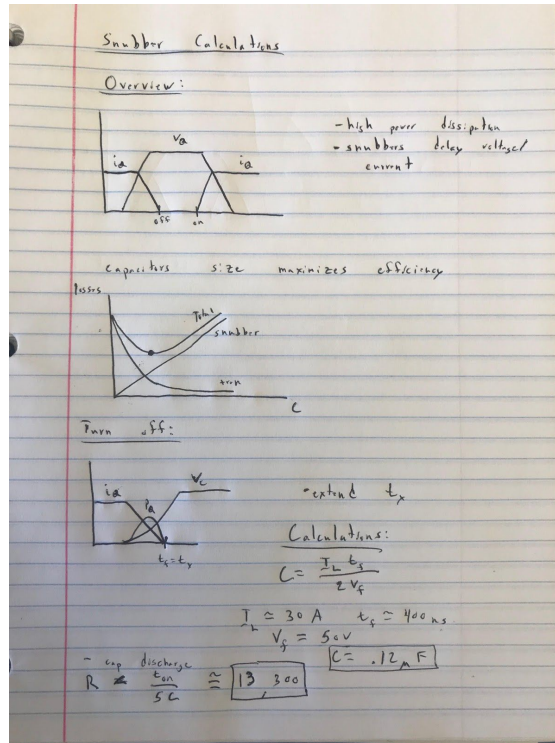


Single leg schematic

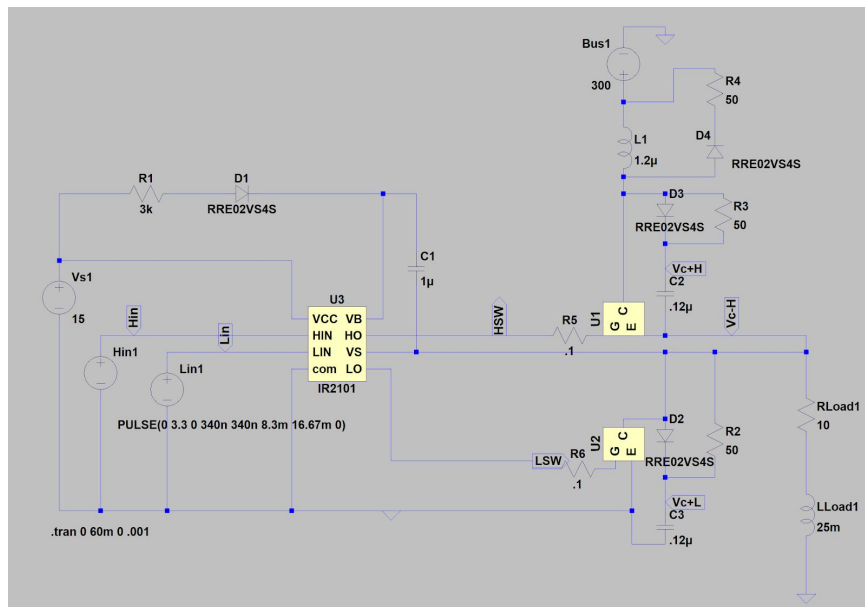


H-Bridge Schematic

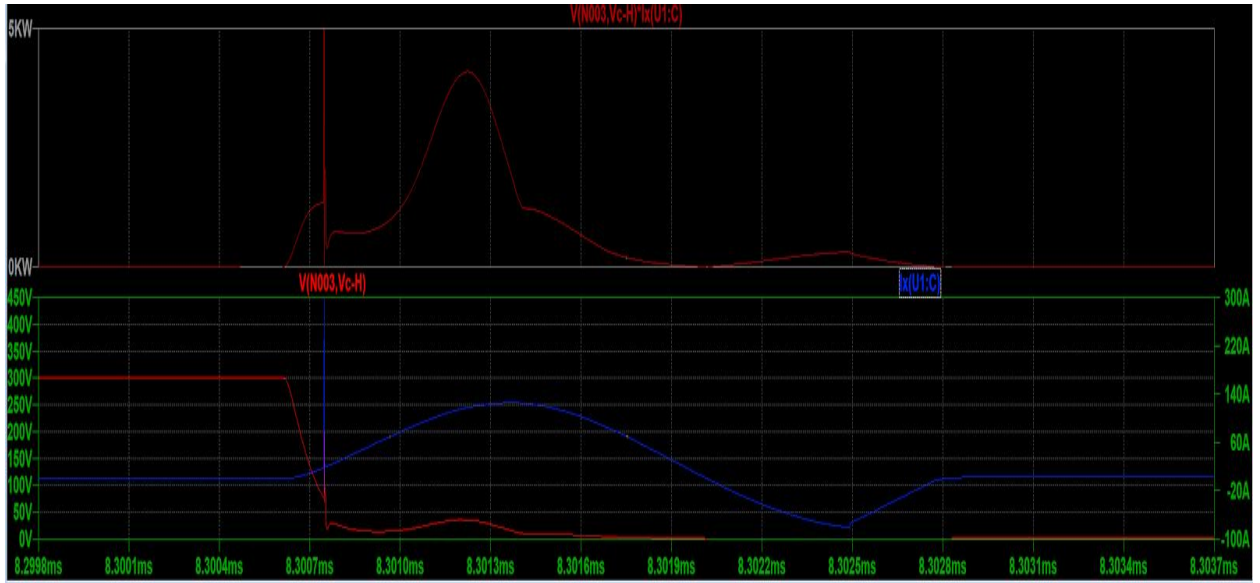
Appendix C (Snubbers)



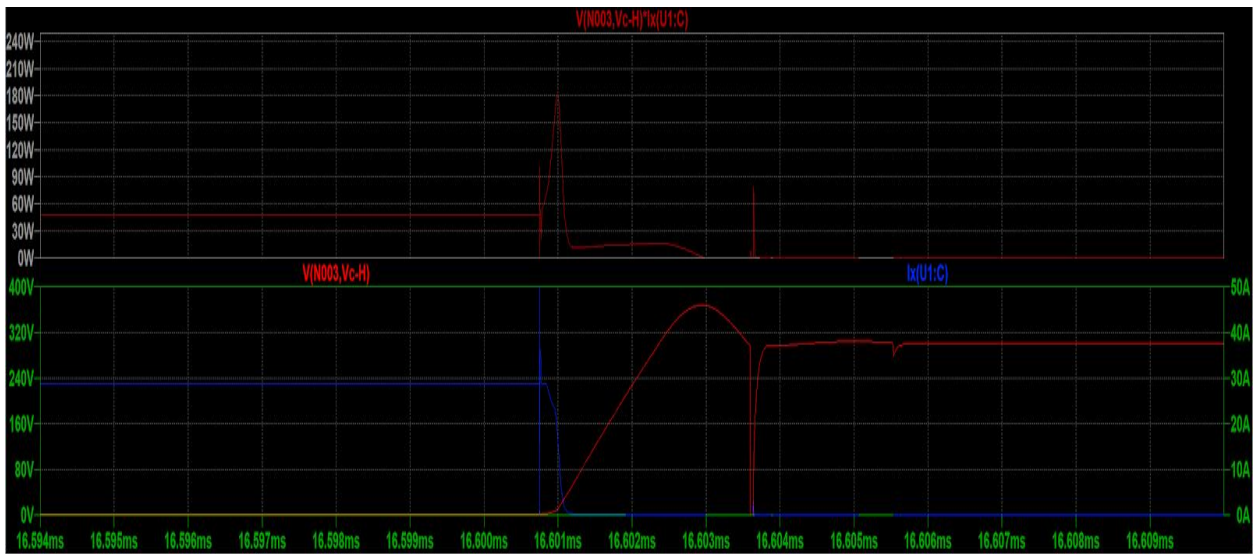
Snubber Calculations



Snubber Schematic

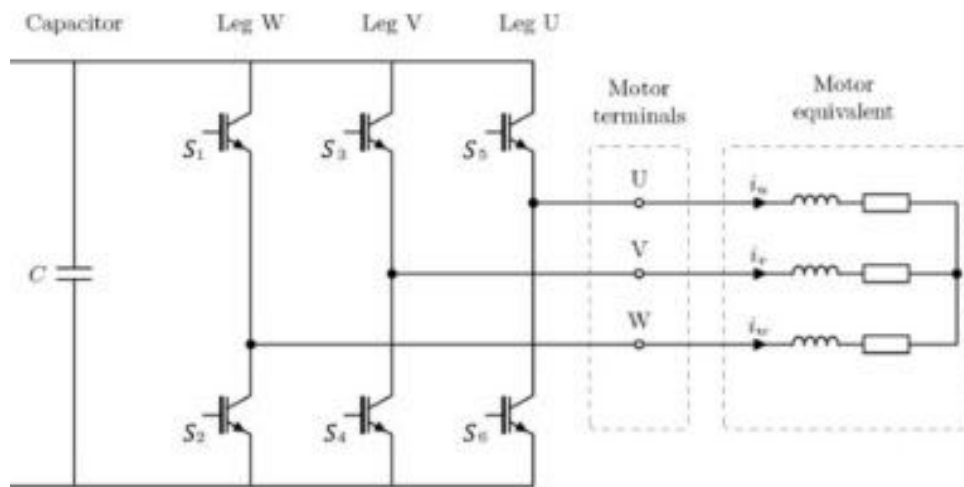


Turn on Snubber Results
(Observing values of Transistor)

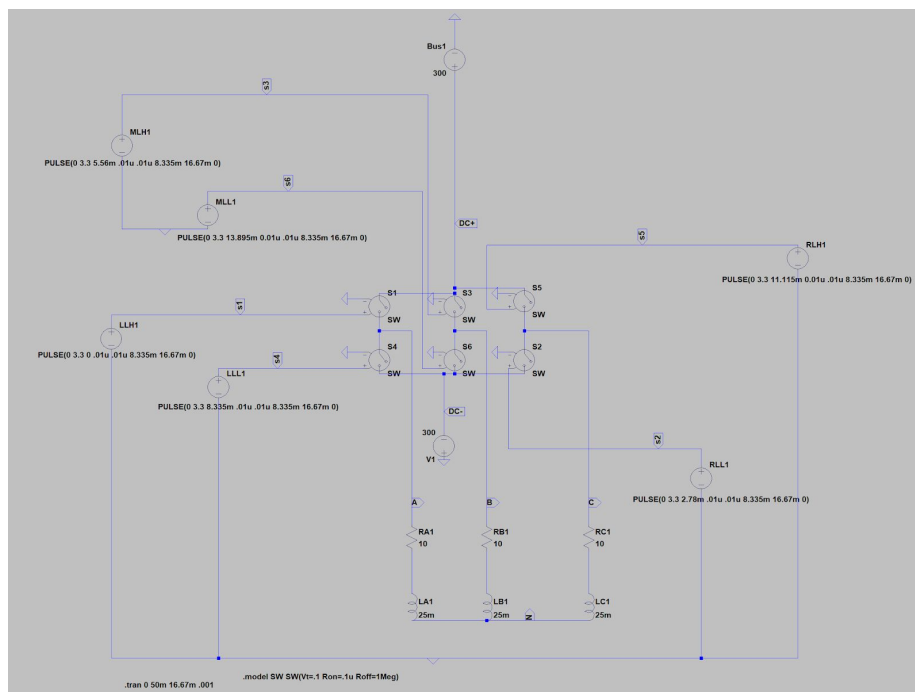


Turn off Snubber Results
(Observing values of Transistor)

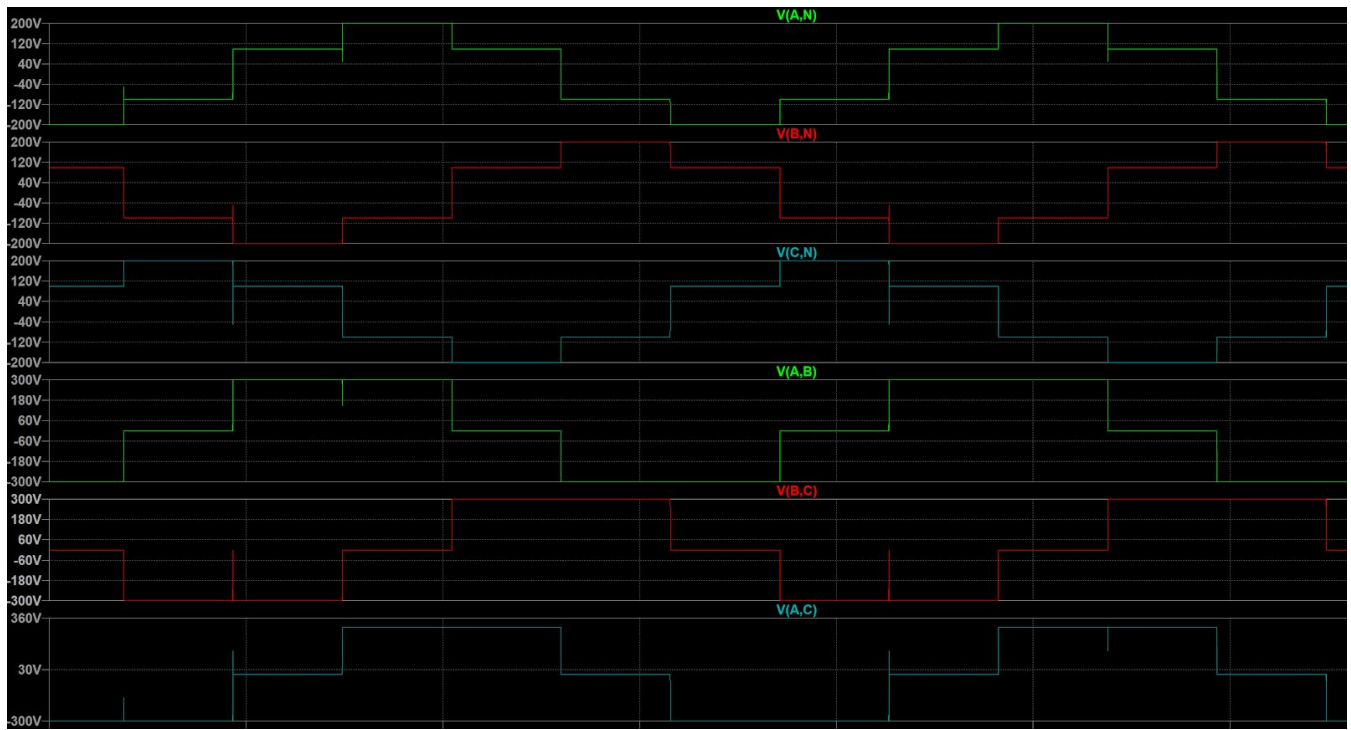
Appendix D (3-phase Inverter)



Basic 3-Phase Inverter Topology

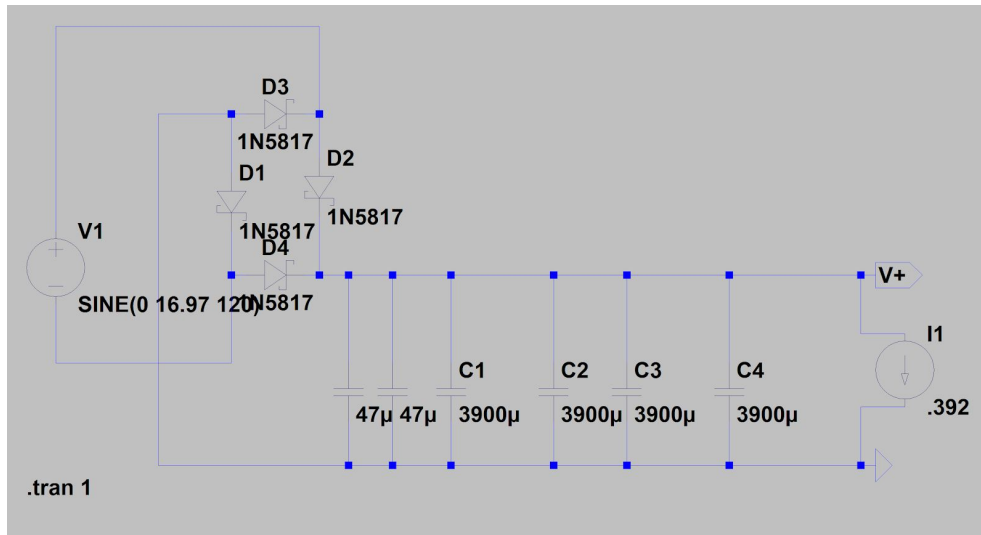


Ideal 3-phase Inverter Schematic for Spice Simulation

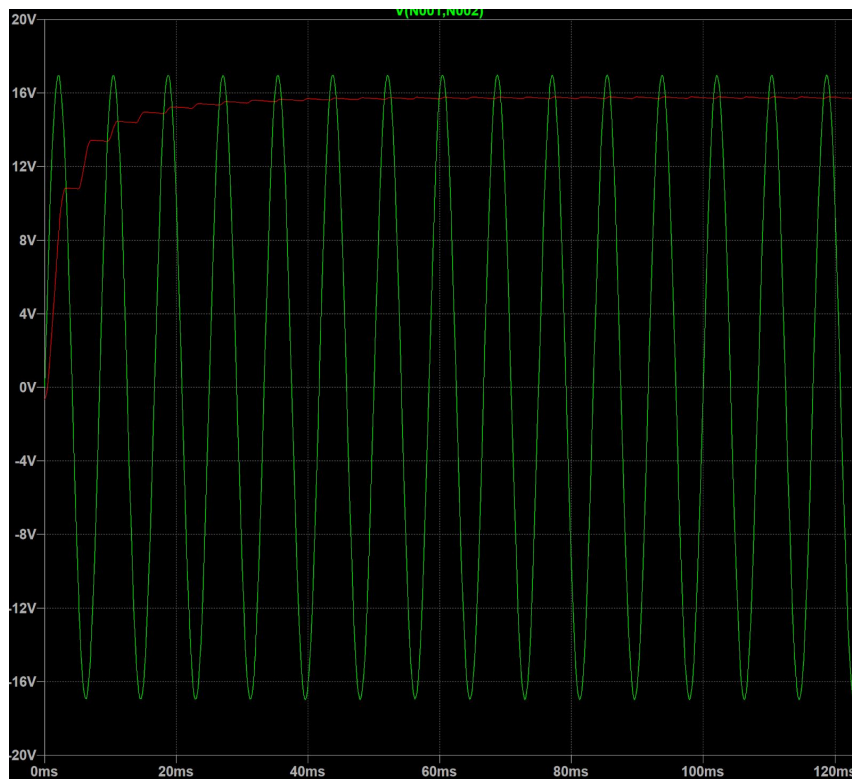


3-Phase Inverter Results

Appendix E (HV power supply)

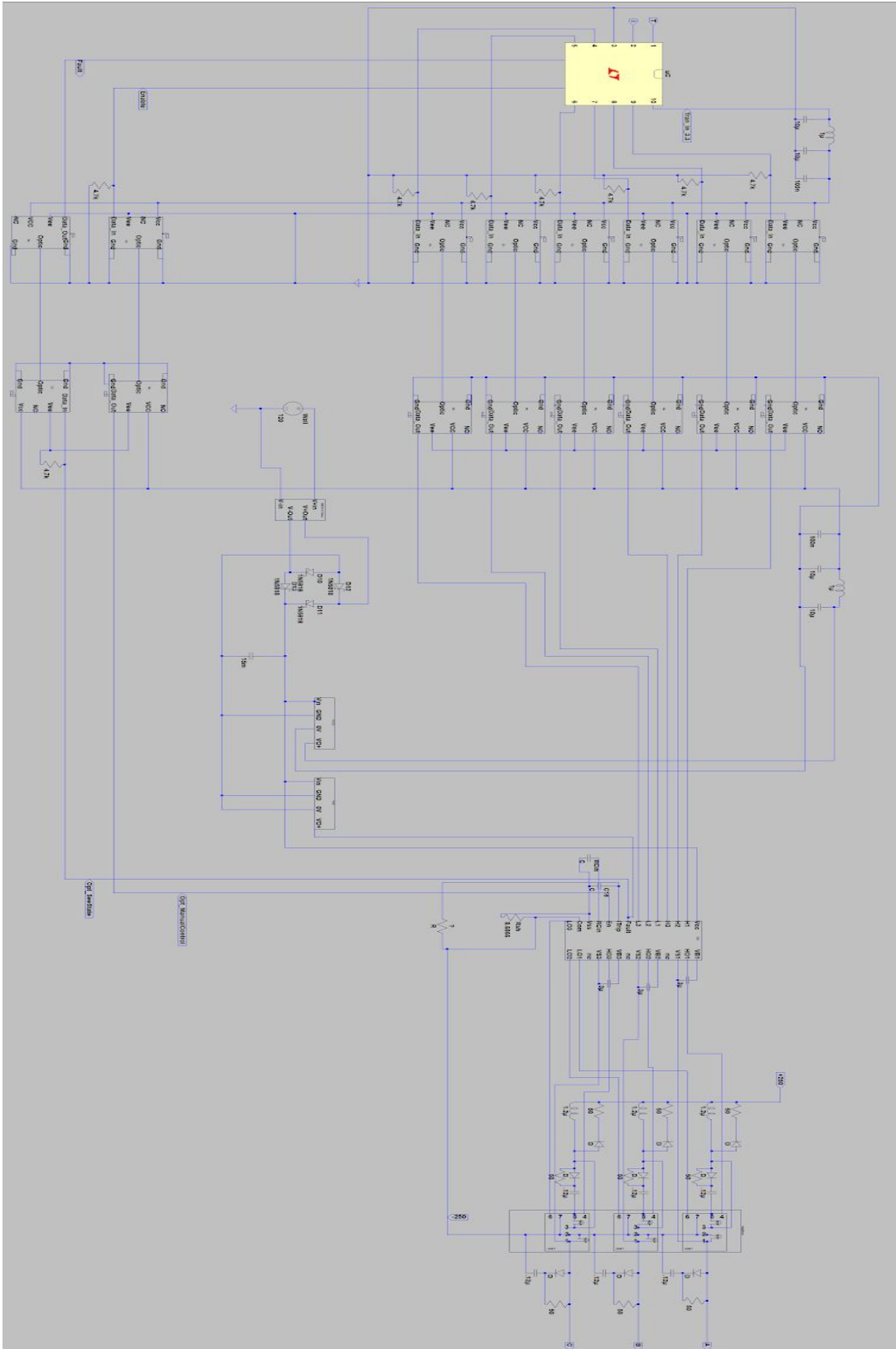


Full Wave Rectifier Schematic



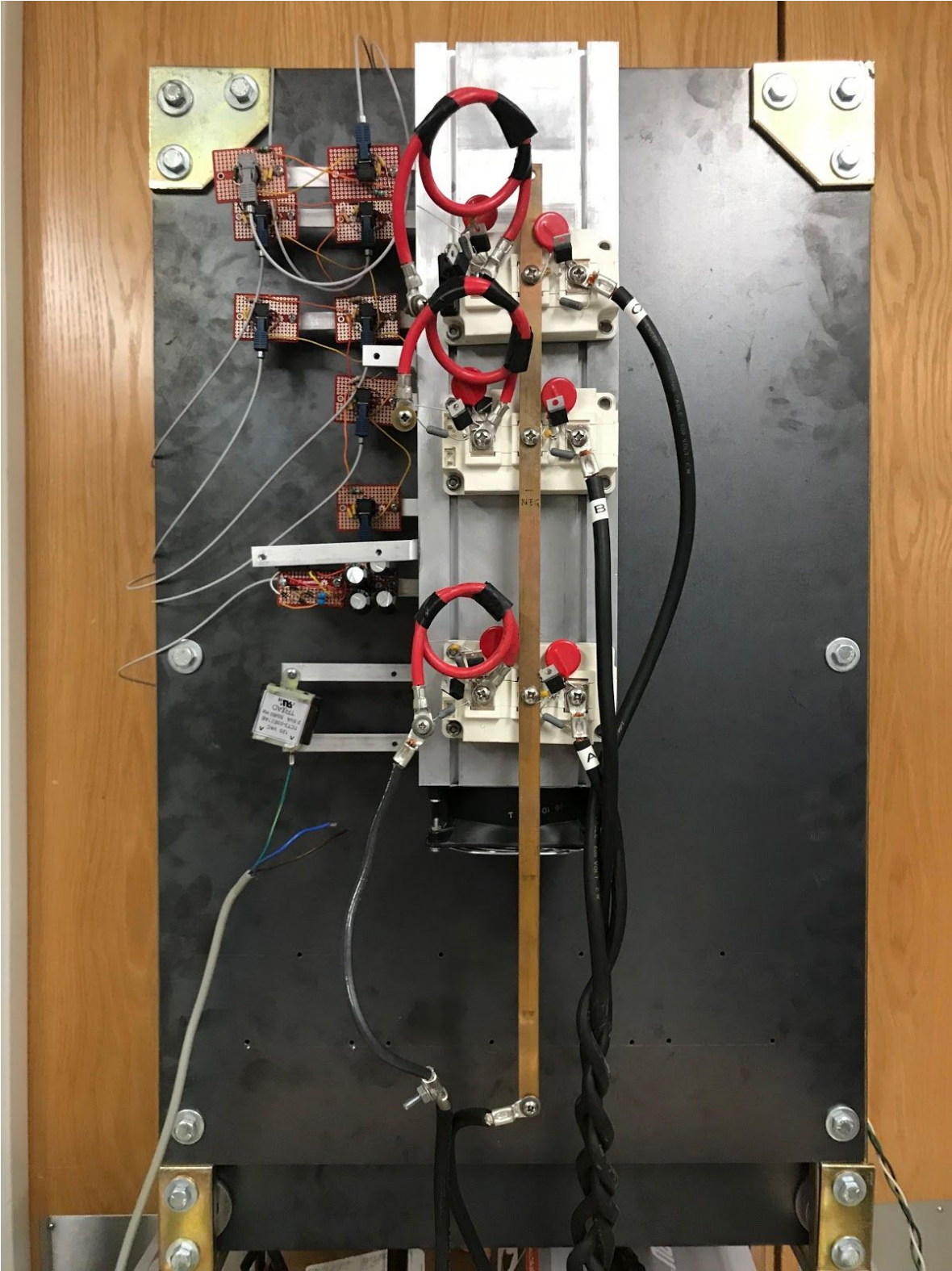
Full Wave Rectifier Simulations Results
(Green=input voltage Red=rectified voltage)

Appendix F (Design Layout)



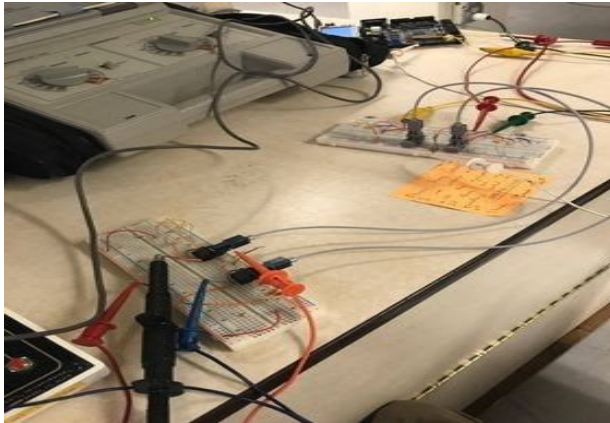
Design Layout

Appendix G (Stand Configuration)

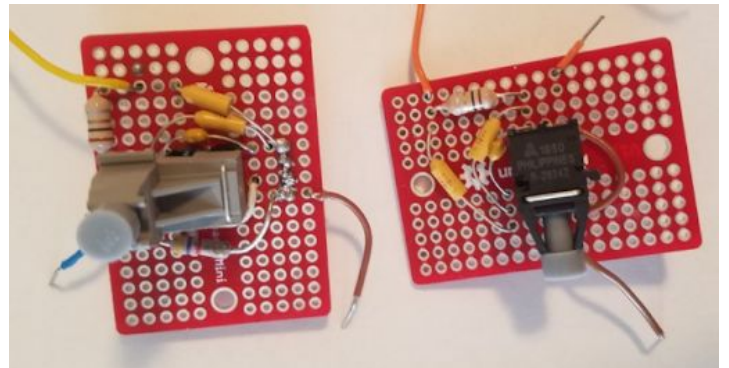


Current Stand Layout (HV side)

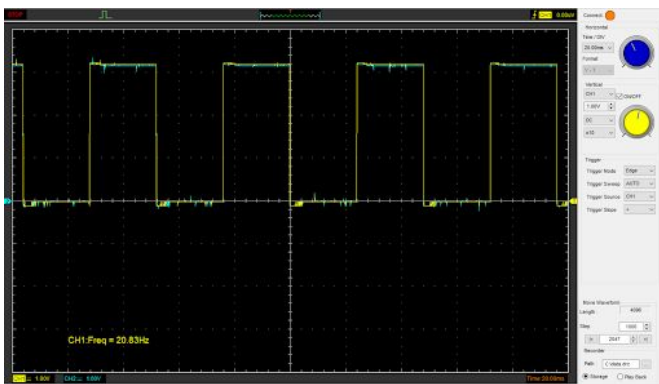
Appendix H (Tests)



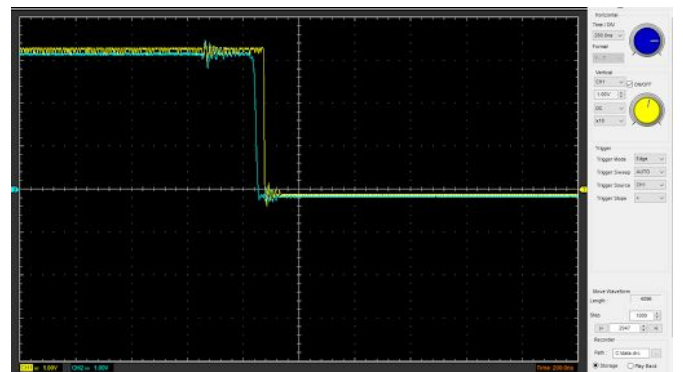
Optics Test Setup



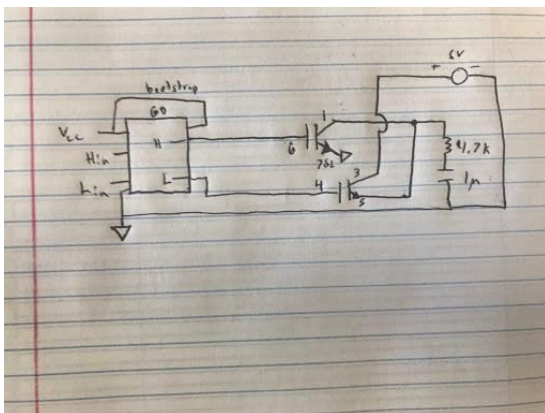
Optic Perfboards
(circuits used for later optics tests)



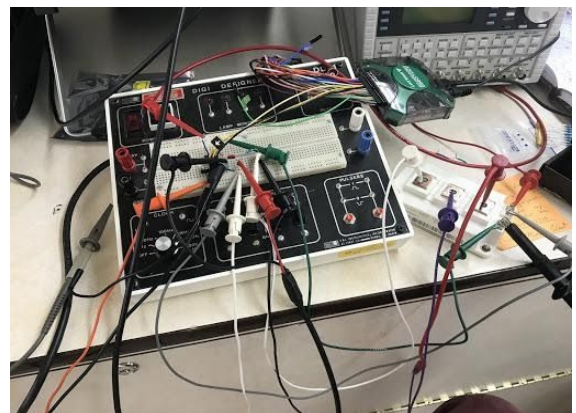
Optic Test Results (full waveform view)



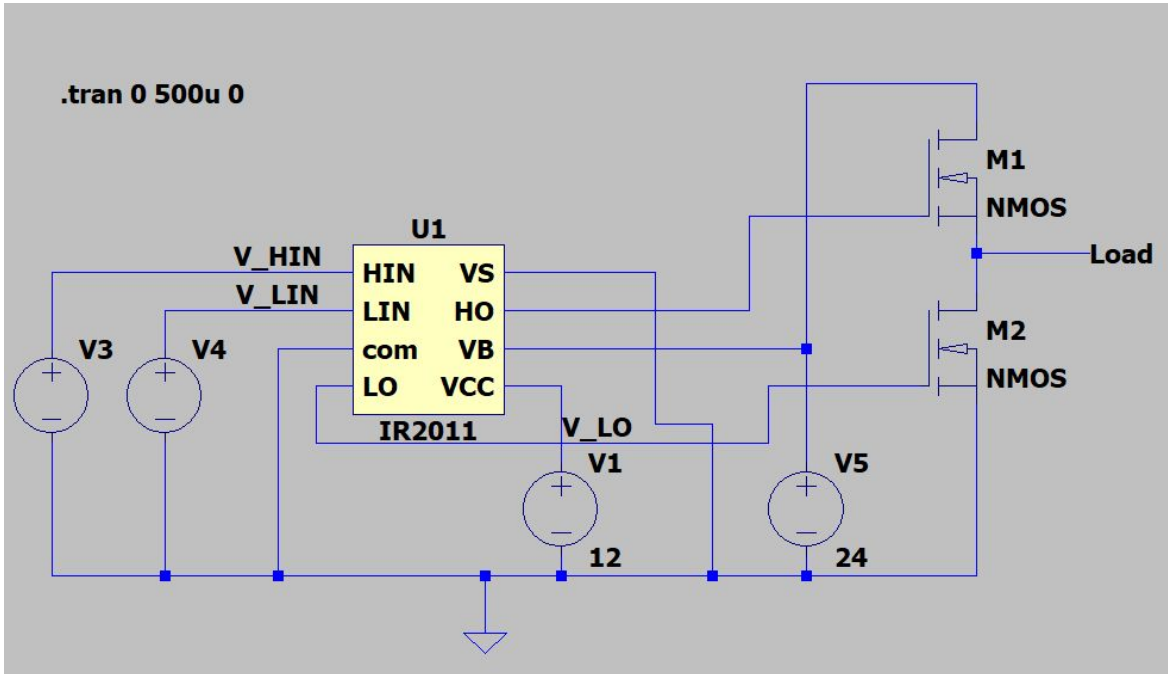
Optic Test Results (delay shown)



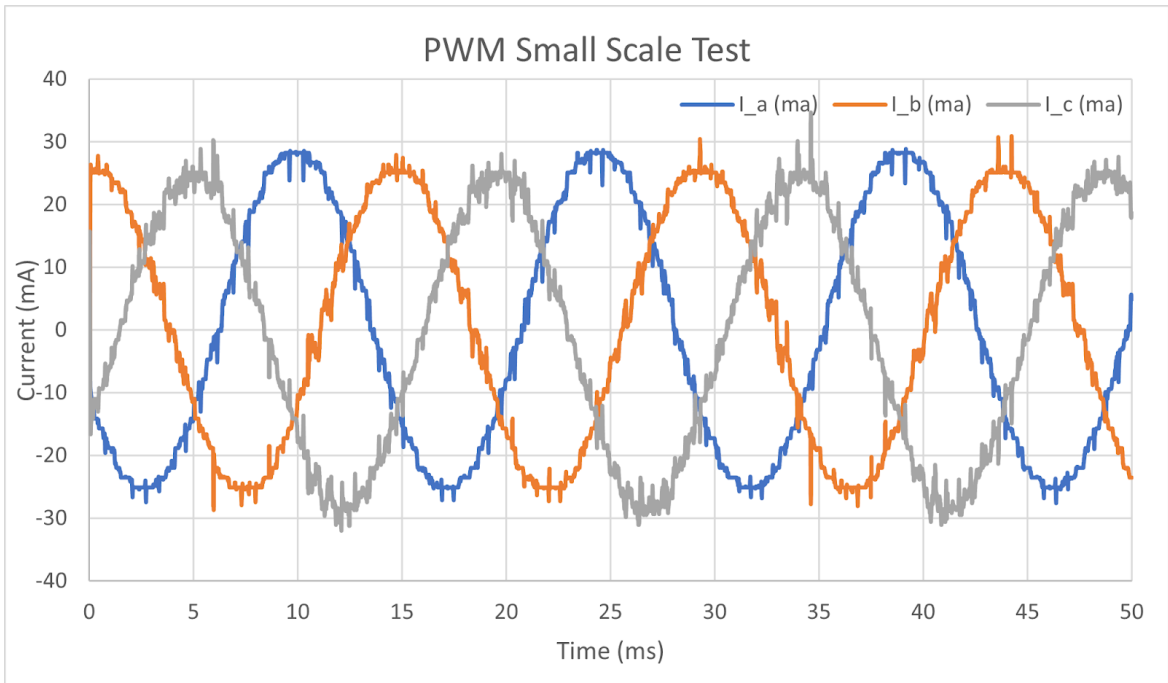
RC Charge Test Schematic



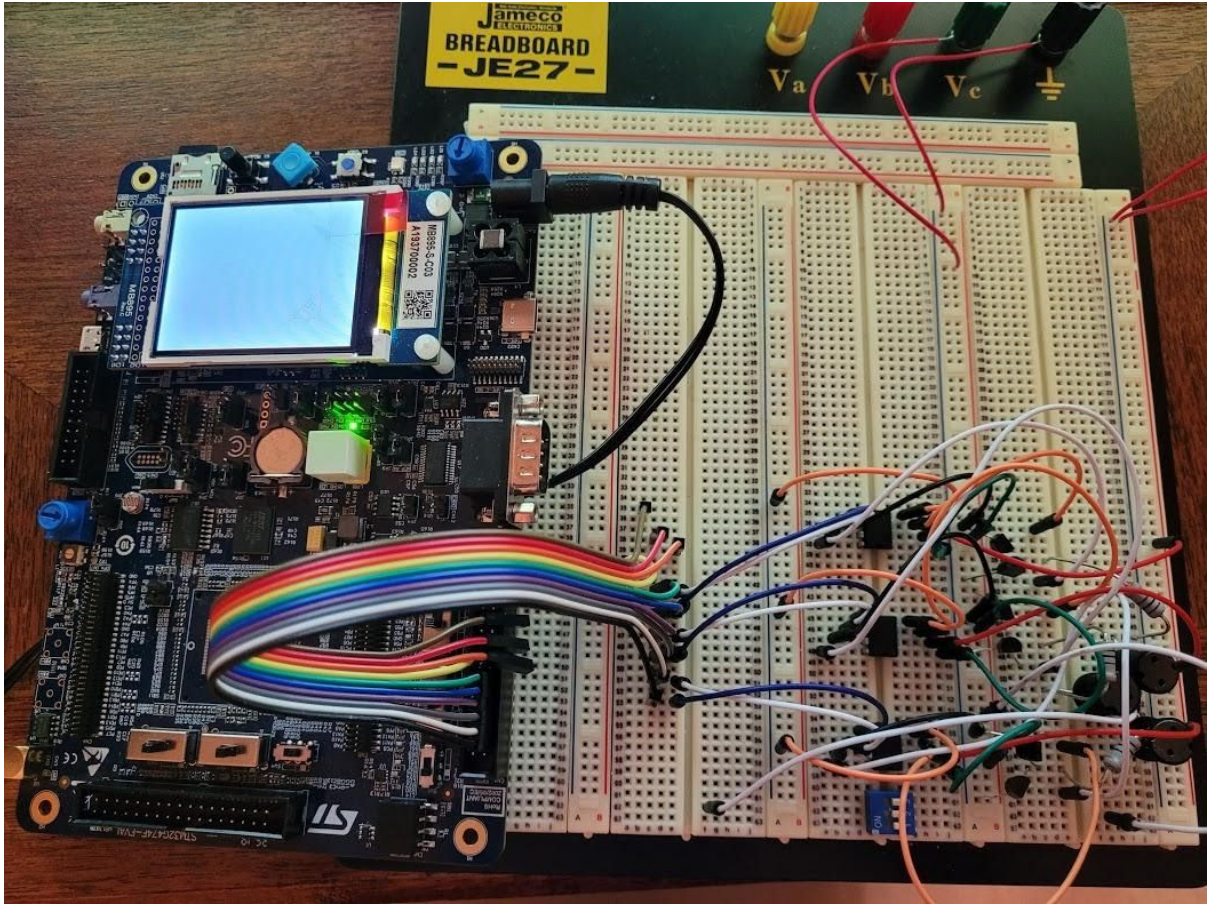
Test Setup for RC Charge Circuit
(testing gate driver and IGBT)



Schematic for a single leg of the PWM small scale test setup. Note that V3 and V4 are the logic outputs from the microcontroller for the high side and low side.

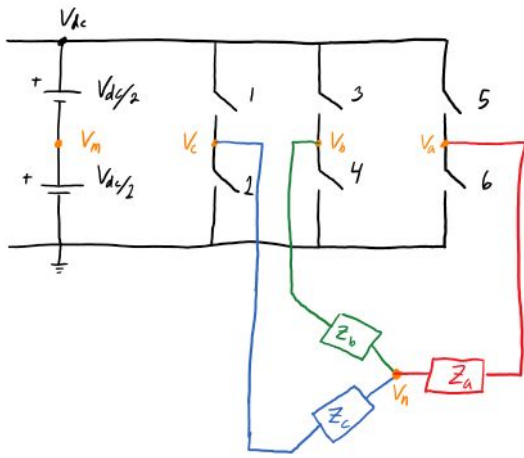


Measured results from full 3-phase PWM small scale test.



The physical circuit used for the PWM small scale tests with Gate drivers, power MOSFETs and a 3-phase R-L load.

Appendix J (Space Vector Modulation)



State	c	b	a
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	0	0
6	1	0	1
7	1	1	1

Even states transition to 7 as the zero-state, odd states use state 0 to ensure fewest switching events

Basic Inverter Model, with state encodings

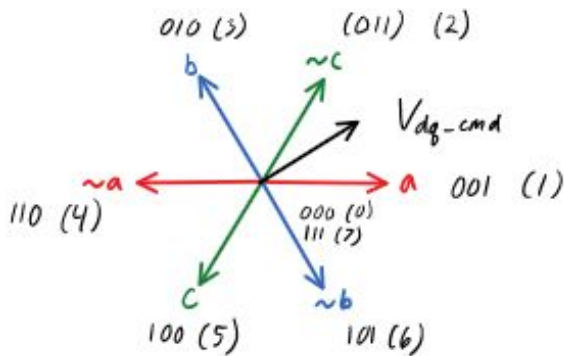
In each cycle, we will have 3 states, 2 non-zero adjacent states and a 0 state.

$$T_0, T_1, T_2$$

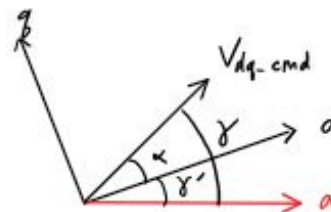
Clearly:

$$T_0 = T_{cycle} - T_1 - T_2$$

The sextant we are in will determine which states are T1 and T2



For the vector shown, we will use states 1 and 2



The desired vector is expressed in dq rotating reference. The reference frame is constantly rotating at an angle gamma prime controlled by the current model. The command vector has a magnitude and phase described in the dq rotating frame at angle alpha from the d axis. The total angle gamma is the sum of gamma prime and alpha and this is the angle used in the space vector algorithm as it is relative to the stationary reference frame.

If we have the two state vectors that we will use as:

$$\vec{V}_{s1}, \vec{V}_{s2}$$

We know that:

$$T_1 \vec{V}_{s1} + T_2 \vec{V}_{s2} = T_{\text{cycle}} \vec{V}_{\text{cmd}}$$

$$\vec{V}_{s1} = \frac{2}{3} \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_{dc}, \quad \vec{V}_{s2} = \frac{2}{3} \begin{bmatrix} \cos 60^\circ \\ \sin 60^\circ \end{bmatrix} V_{dc} \quad \text{For first sextant}$$

$$T_1 V_{dc} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \frac{2}{3} + T_2 V_{dc} \begin{bmatrix} \cos 60^\circ \\ \sin 60^\circ \end{bmatrix} \frac{2}{3} = T_{\text{cycle}} V_{\text{cmd-mag}} \begin{bmatrix} \cos \delta \\ \sin \delta \end{bmatrix}$$

Solving, we obtain:

$$T_1 = \frac{T_{\text{cycle}} V_{\text{cmd-mag}} \sin(60^\circ - \delta)}{\frac{2}{3} V_{dc} \sin(60^\circ)}$$

$$T_2 = \frac{T_{\text{cycle}} V_{\text{cmd-mag}} \sin(\delta)}{\frac{2}{3} V_{dc} \sin(60^\circ)}$$

In general:

$$T_1 \left(\frac{2}{3} V_{dc}\right) e^{i(n-1)\pi/6} + T_2 \left(\frac{2}{3} V_{dc}\right) e^{i(n)\pi/6} = T_{\text{cycle}} V_{\text{cmd-mag}} e^{i\delta}$$

Which leads to:

$$T_1 = K \sin(n\pi/3 - \delta)$$

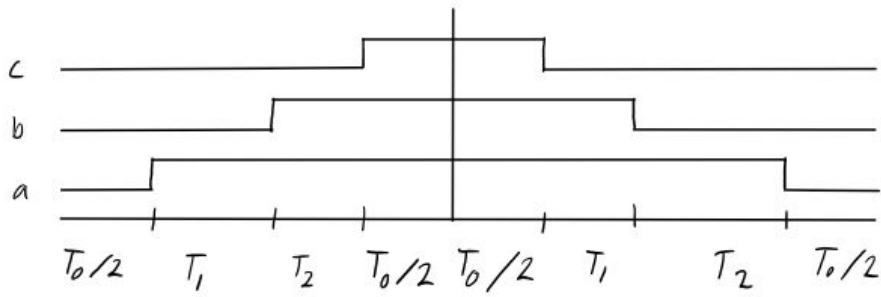
$$T_2 = K \sin(\delta - (n-1)\pi/3)$$

$$T_0 = T_{\text{cycle}} - T_1 - T_2$$

$$K = \frac{\sqrt{3} T_{\text{cycle}} V_{\text{cmd-mag}}}{V_{dc}}$$

These are the final formulas used to calculate the switching times in the simulation and the final code

Using Center-Aligned PWM, the waveform generated will be like the following (note that every cycle contains 2 mirrored versions as the period register counts up and then down for center aligned PWM)



$$S_1 = 001 \quad (\text{state 1})$$

$$S_2 = 011 \quad (\text{state 2})$$

Period Register Settings:

$$P_1 = (S_1[2] * T_1 + S_2[2] * T_1 + T_0/2)$$

$$P_2 = (S_1[1] * T_1 + S_2[1] * T_1 + T_0/2)$$

$$P_3 = (S_1[0] * T_1 + S_2[0] * T_1 + T_0/2)$$