

Minutes for Senior Design
Team New Perspective Weekly Meeting
Sept. 17th, 2013

See Agenda For the week for topic overview:

What are our data rates gonna be?

- Image sensor trapezoidal
- We build FPGA that processes the image
- Get the digital image – could be only one bit (car or road)

How to process the image of the car (how to identify)

- Run an edge detection algorithm
- Run a fill algorithm for the car's area
- Calculate the center of the car's area
- Background level needs to be extracted
- Feedback into FPGA (can adjust gain, or whatever to end up with same level from sensor)
- Possibly going to send only object edge to FPGA rather than whole image

Have a line memory on chip

- Do a digital comparison on chip
- Just stream out moving object to Chip
- Would occasionally need to send six bits of data to extract average road conditions or something

Compare multiple rows at a time

- Compare 8 rows of previous data to current data
- Done in imager or can be done in FPGA
- Would be nice to enable or disable that feature
- Can even have a kernel there to see which edges to fill between

What is going to be done on the chip and off the chip

- To be safe, we need to shift in frame average on chip no matter what
- We can enable and disable that feature easily and just give background subtracted image
- Somehow we need to subtract the average value (on or off trip)
- We are going to do similar to manufacturing line (detect packages, fill them, find center, count)

Maybe we should build an SSLAR2 camera and do whatever we want to do with that sensor

- Eliminates data rate problems completely
- Can use either upper or lower four bits or whatever
- In a controlled environment we can use that chip to find center of objects

Action Item: look at SSLAR2 camera development by November and run some of the codes
Look at books on machines

Maybe have at least 4 bits to see 16 different grey levels – output not imager itself
Speed – 100-200 frames per second.

Frame to frame variation will not be that big

Do we need to have an ideal condition for this project?

No. We will use ideal conditions in a lab and then add defects over time

At some point we may do a field try. The point at which we are confident it'll at least work some of the time

If we had working algorithms that we could show would work would that be a good thing for the snapshot in December?

Yes. We could even use C or C++, sample video and MatLab Code, use SSLAR2.

If we don't end up doing that what could we do?

Use a video program to run through SSLAR2

MatLab have an import video function

Had a grad student implement MatLab SSLAR code ([get code](#))

Currently using DLPS HS FPGA2

Possibly use same FPGA but next model

Or we could possibly develop new FPGA board? We need to get it populated by some other company. Can solder FPGA's ourselves.

Get a new board with old SSLAR2 on it

We also have two SSLAR boards with old virtex's on them may still work.

Use SRAM instead of SDRAM

Need a 4 layer board for FPGA's

Need new somewhat descriptive team name

Dropbox is fine for stuff

Set up gmail with email address and forwarding to all

What we need to be working on this week

Get SSLAR2 camera working and get raw data feed from it

Get keys from Arleen for lab GJ 206

Get access to computers (usernames, etc.)

Scholarships are for us not for the project