

Problem Statement

Develop a system to display HDMI video on an array of LED panels.



HDL Design Overview

Programming the FPGA involves four primary modules: HDMI Decoder: Receives pixel data from an external HDMI source and performs lane deskew and clock alignment. EDID (Extended Display Identification Data) is used to help HDMI sources identify the panel array as an actual display.

Image Buffer:

Image Scaler: LED Control:

Tracks the horizontal and vertical synchronization signals from the HDMI Decoder to determine frame boundaries and stores the pixel data into a temporary buffer as it is received. Scales the video frames from a 640x480 input image to a 64x64 output image. Receives the scaled frame images and sends output signals to the LED panels. Performs gamma correction on the image and outputs full 24-bit color using pulse width modulation.





LED Control Module

The LED panels have twelve input pins: two sets of RGB pins, four address pins, three ground pins, and clock, latching, and blanking pins. Pixel data is shifted once for each row using the address and latch signals.

The panels can be chained together so that longer rows of pixel data can be shifted, which allows a larger image to be displayed using multiple panels. To achieve full 24-bit color, we employed a pulse width modulation strategy.



implement pulse width modulation.

Future Work

ATLYS FPGA: Panel Array: Image Scaler:

Color Correction: Color correction could be improved.

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There are a number of opportunities for improvement, economization, and expansion for this project:

A less expensive FPGA could be used.

Expand the number of panels beyond a 2x2 array.

Improve the quality of the image scaling by using a more advanced interpolation method on the FPGA.

Team Members

Faculty Advisors

Robert Rinker – Sponsor Bruce Bolden – Mentor

Past Team Member (Fall 2014)

Alex Eklund – Computer Science







