

Meeting Minutes – November 14th, 2013

University of Idaho, Team New Perspective

Back up Plan Stuff

- The deadline for the chip to be taped out is November 22nd – not going to happen
- The pixels are done – the supporting electronics are not done yet
- The fab that we are using changed their technology files
 - Need to download new technology files and make sure there are no new errors – going to take quite a bit of time
- Spent some time showing John's teacher what the project is
- Will now tape out in January and get the chip back in April

Actual Plans

- Will be using SSLAR2

Mock Road

- Need to be able to control the speed of the car and measure how fast it is going compared to what we are measuring it going at
- Potentially use some kind of motor to pull the car, photogates to measure the speed, something that accurately measures
- Get 10-20 photo gates for the project
- Prolly need 10 feet for testing – Maybe could use five feet at expo?
- Maybe use real footage of cars going by the SUB
- What does John need to know
 - Using PIC microcontrollers
 - Use fishing wire to pull the car
 - Maybe use BRIO trains instead of Hot Wheels Cars
 - Awesome Idea

Give John Goals and what he will learn, Have John at the level to present the second week in January

- Read PIC 32 MicroController book and do sections of code
- Understand Scaling and Geometry

Questions about the SSLAR2

- What are the registry definitions for the SSLAR2
- Not sure how to increase the frame rate
 - Increase clock signal and ramp up

- Increase the Threshold
 - Prolly the maximum frame rate is 20 fps?
- Keep the jump rate at 4 or 8 otherwise it'll slow us down
- When we increase the clock frequency the light integration time is much less and we'll need to increase the gain
- All these controls are in the SSLAR2?
 - The step is in the SSLAR
 - Used by engine and event detector (just a comparator)
 - Threshold is used to detect event
 - Step is used by (controls) the counter to know how many steps it goes
 - The threshold is in the FPGA for SSLAR2
 - Threshold used to generate DAC
 - DAC is used to compare to column
 - Triggers something in the engine to say fall back or continue moving step by step
 - Row addressing logic is just a shift register on SSLAR2
 - Clk and input are set by FPGA
 - On FPGA we can set the input channel by clocking multiple CLK's between rows
 - CLK signals
 - One controls Row
 - One controls ADC
 - One control ramp
- To speed up the chip, make the threshold 32 or even 64
 - We can jump forward and then go back and jump back by half?
 - There is a jump signal coming out from the event detector
 - Jump is prolly used to tell when we're are going