

## ## Meeting Minutes

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\*Client\*

\*March 7, 2018 1:30pm-1:45pm\*

## ### Agenda Notes/Status Reports

Status: Currently we have reworked the ADC design and it now builds and uploads to the board. We are then able to configure the ADC core via a modified software driver and ensure the values are written correctly. However, it is not passing the self test, it appears to be an issue with the jesd204b link. We think it may be a software configuration issue.

For the antenna, the range of critical frequencies is between 1-250MHz, which is difficult to design an antenna for as it would have a large diameter and not well directed at the processor. It may be easier to use an antenna that captures a large bandwidth including higher frequencies, and then use a filter to get the desired range. The Pulse Larsen antenna would be able to perform this task, which is about \$50.

No update with the algorithm. We plan to work on alignment issues of the algorithm after spring break.

## ### Key Decisions

\* The throughput of Ethernet connection is 80 megabits per second, with 100 megabytes of data, the transfer will take about 10 seconds.

\* No meeting next week due to Spring Break!

## ### Action Items

\* Team: Produce table of groupings of instructions of what we can and cannot distinguish from (once we get accurate hardware captures)

\* Team: Build and verify FPGA design.