

AGENDA – Oct. 3rd, 2013

Action Items

Snapshot Presentation: Show what we have so far

Show our definition sheet for terms thus far and discuss

Discussion

What do we need to do for the chip to be able to have a variable number of trip wires for that method yet also image and process the whole chip?

Delta cap issues: the delta cap that we have at a decently high frame rates might still be too much...so...possible fix would be only looking at a certain number of frames (every second or third?) Every eight frames we go to the delta cap or keep a rolling average to change the delta cap based off that average

Data Rate Problems: the problem is not necessarily getting the data into the FPGA, it is processing the data. Thus we might as well take all the data from the chip and then select what part of it we want to use

Talk about an on-chip buffer so that we get a rather constant data rate?

Talk about difference between threshold and cap

Talk about frame rate for Dr. Ay to design chip – 10 ms

Error introduced by frame rate....See PowerPoint for number and calculation methods

We are unable to get sub-pixel accuracy, thus we might as well lower the frame rate?

Will we dictate our own frame rate? Be able to pull out the data as fast as we want?