Ideal Op Amp Circuits

The operational amplifier, or op amp as it is commonly called, is a fundamental active element of analog circuit design. It is most commonly used in amplifier and analog signal processing circuits in the frequency band from 0 to 100 kHz. High-frequency op amps are used in applications that require a bandwidth into the MHz range. The first op amps were vacuum-tube circuits which were developed for use in analog computers. Modern op amps are fabricated as integrated circuits that bare little resemblance to the early circuits. This chapter covers some of the basic applications of the op amp. It is treated as an ideal circuit element without regard to its internal circuitry. Some of the limitations imposed by non-ideal characteristics are covered in the following chapter.

The notation used here is as follows: Total quantities are indicated by lower-case letters with upper-case subscripts, e.g. v_I, i_O, r_{IN}. Small-signal quantities are indicated by lower-case letters with lower-case subscripts, e.g. v_i, i_o, r_{out}. Transfer function variables and phasors are indicated by upper case letters and lower-case subscripts, e.g. V_i, I_o, Z_{in}.

1.1 The Ideal Op Amp

The *ideal op amp* is a three terminal circuit element that is modeled as a voltage-controlled voltage source. That is, its output voltage is a gain multiplied by its input voltage. The circuit symbol for the ideal op amp is given in Fig. 1.1(a). The input voltage is the difference voltage between the two input terminals. The output voltage is measured with respect to the circuit ground node. The model equation for the output voltage is

$$v_O = A\,(v_+ - v_-) \tag{1.1}$$

where A is the voltage gain, v_+ is the voltage at the non-inverting input, and v_- is the voltage at the inverting input. The controlled source model of the ideal op amp is shown in Fig. 1.1(b).

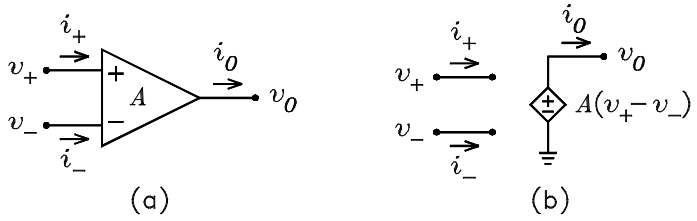

Figure 1.1: (a) Op-amp symbol. (b) Controlled-source model.

The terminal characteristics of the ideal op amp satisfy four conditions. These are as follows:

1. The current in each input lead is zero.
2. The output voltage is independent of the output current.

3. The voltage gain A is independent of frequency.

4. The voltage gain A is very large, approaching infinity in the limit.

The first condition implies that the resistance seen looking into both input terminals is infinite. The second implies that the voltage gain is independent of the output current. This is equivalent to the condition that the output resistance is zero. The third implies that the bandwidth is infinite. The fourth implies that the difference voltage between the two input terminals must approach zero if the output voltage is finite.

For it to act as an amplifier, the op amp must have feedback applied from its output to its inverting input. That is, part of the output voltage must be sampled by a network and fed back into the inverting input. This makes it possible to design an amplifier so that its gain is controlled by the feedback network.

To illustrate how feedback affects the op amp, consider the circuits shown in Fig. 1.2. The networks labeled N_1 and N_F, respectively, are the input and feedback networks. The op amp of Fig. 1.2(a) has positive feedback whereas the op amp of Fig. 1.2(b) has negative feedback. Let a unit step of voltage be applied to the input of each circuit at $t = 0$. The arrows in the figures indicate the directions in which the input voltages change, i.e. each input voltage increases. For the circuit of Fig. 1.2(a), the voltage increase at v_i is fed through the N_1 network to cause the voltage to increase at the v_+ terminal. This is amplified by a positive gain $(+A)$ and causes the output voltage to increase. This is fed back through the N_F network to further increase the voltage at the v_+ terminal. (The arrow for the feedback voltage is enclosed in parentheses to distinguish it from the arrow for the initial increase in voltage.) This causes the output voltage to increase further, causing v_+ to increase further, etc. It follows that the circuit is not stable with positive feedback.

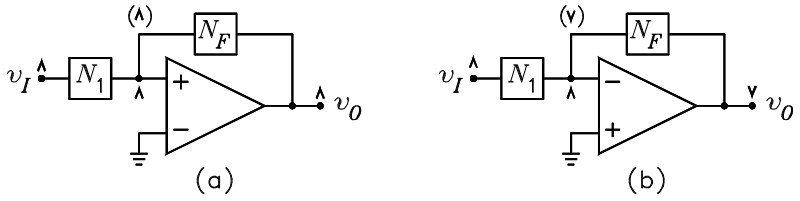

Figure 1.2: (a) Op amp with positive feedback. (b) Op amp with negative feedback.

For the circuit of Fig. 1.2(b), the voltage increase at the input is fed through the N_1 network to cause the voltage to increase at the v_- terminal. This is amplified by a negative gain $(-A)$ and causes the output voltage to decrease. This is fed back through the N_F network to cause the voltage at the v_- input to decrease, thus tending to cancel the initial increase caused by the input voltage. Because the v_- voltage is decreased by the feedback, it follows that v_O is decreased also. Thus the circuit is stable.

When negative feedback is used in an op amp circuit, the feedback tends to force the voltage at the v_- input to be equal to the voltage at the v_+ input. It is said that a *virtual short circuit* exists between the two inputs. A virtual short circuit between two nodes means that the voltage difference between the nodes is zero but there is no branch for a current to flow between the nodes. There is no virtual short circuit between the v_- and v_+ inputs to an op amp which has positive feedback. If it has both negative and positive feedback, the virtual short circuit exists if the negative feedback is greater than the positive feedback.

We have used the concept of signal tracing in the circuits of Fig. 1.2 to illustrate the effects of feedback. Signal tracing is a simple concept which can be applied to any circuit to check for positive and negative feedback. Circuits which have positive feedback are unstable in general and are not used for amplifier circuits. With few exceptions, the circuits covered in this chapter have only negative feedback.

1.2 Inverting Amplifiers

1.2.1 The Inverting Amplifier

Figure 1.3(a) shows the circuit diagram of an inverting amplifier. The input signal is applied through resistor R_1 to the inverting op amp input. Resistor R_F is the feedback resistor which connects from the the output to the inverting input. The circuit is called an inverting amplifier because its voltage gain is negative. This means that if the input voltage is increasing or going positive, the output voltage will be decreasing or going negative, and vice versa. The non-inverting input to the op amp is not used in the inverting amplifier circuit. The figure shows this input grounded so that $v_+ = 0$.

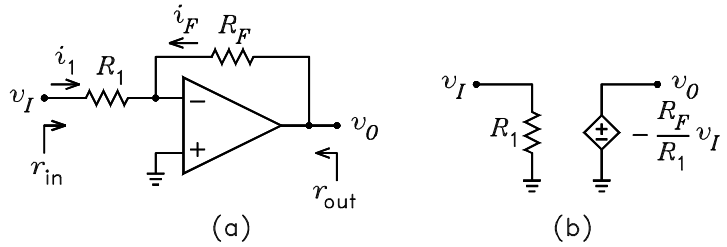

Figure 1.3: (a) Inverting amplifier. (b) Controlled-source model.

For the circuit of Fig. 1.3(a), the voltage at the inverting input is given by $v_- = -v_O/A$. For v_O finite and $A \to \infty$, it follows that $v_- \to 0$. Even though the v_- input is not grounded, it is said to be a virtual ground because the voltage is zero, i.e. at ground potential. Because $i_- = 0$, the sum of the currents into the v_- node through resistors R_1 and R_F must be zero, i.e. $i_1 + i_F = 0$, where $i_1 = v_I/R_1$ and $i_F = v_O/R_F$. Thus we can write

$$i_1 + i_F = 0 \qquad \Longrightarrow \qquad \frac{v_I}{R_1} + \frac{v_O}{R_F} = 0 \tag{1.2}$$

This relation can be solved for the voltage gain to obtain

$$\frac{v_O}{v_I} = -\frac{R_F}{R_1} \tag{1.3}$$

The input resistance is calculated from the relation $r_{in} = v_I/i_1$. Because $v_- = 0$, it follows that

$$r_{in} = R_1 \tag{1.4}$$

The output resistance is equal to the output resistance of the op amp so that

$$r_{out} = 0 \tag{1.5}$$

The controlled source model of the inverting amplifier is shown in Fig. 1.3(b).

Example 1 *Design an inverting amplifier with an input resistance of* $2\,\text{k}\Omega$*, an output resistance of* $100\,\Omega$*, and an open-circuit voltage gain of* -30 *(an inverting decibel gain of* $29.5\,\text{dB}$*).*

Solution. The circuit diagram for the amplifier is given in Fig. 1.4(a). For an input resistance of $2\,\text{k}\Omega$, Eq. (1.4) gives $R_1 = 2\,\text{k}\Omega$. For a voltage gain of -30, it follows from Eq. (1.3) that $R_F = 60\,\text{k}\Omega$. For an output resistance of $100\,\Omega$, the resistor $R_O = 100\,\Omega$ must be used in series with the output as shown in the figure.

Example 2 *Calculate the voltage gain of the circuit of Fig. 1.4(a) if a* $1\,\text{k}\Omega$ *load resistor is connected from the output to ground. The circuit with the load resistor is shown in Fig. 1.4(b).*

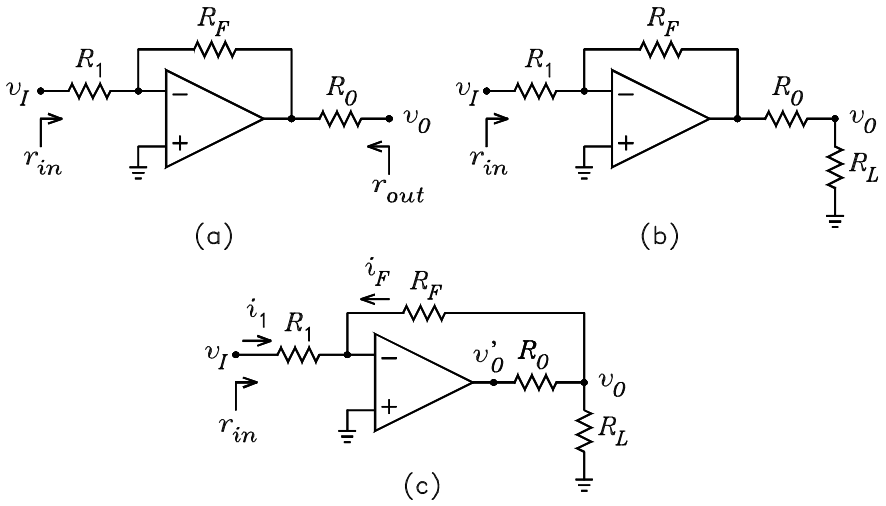

Figure 1.4: (a) Circuit for Example 1. (b) Circuit for Example 2. (c) Circuit for Example 3.

Solution. The voltage gain decreases when R_L is added because of the voltage drop across R_O. By voltage division, the gain decreases by the factor

$$\frac{R_L}{R_O + R_L} = \frac{1000}{1000 + 100} = \frac{10}{11}$$

It follows that the loaded voltage gain is $(10/11) \times (-30) = -27.3$ (an inverting decibel gain of 28.7 dB).

Example 3 *For the inverting amplifier circuit of Fig. 1.4(b), investigate the effect of connecting the feedback resistor R_F to the load resistor R_L rather than to the op amp output terminal. The modified circuit is shown in Fig. 1.4(c).*

Solution. Because $i_1 + i_F = 0$, it follows that $v_I/R_1 + v_O/R_F = 0$. This gives the voltage gain $v_O/v_I = -R_F/R_1$. Because this is independent of R_L, it follows that the output resistance of the circuit is zero. Thus the circuit looks like the original circuit of Fig. 1.4(b) with $R_O = 0$. With $R_O \neq 0$, the op amp must put out a larger voltage in order to maintain a load voltage that is independent of R_O. Let v_O' be the voltage at the op amp output terminal in Fig. 1.4(c). By voltage division, the output voltage is given by

$$\frac{v_O}{v_O'} = \frac{R_L \| R_F}{R_L \| R_F + R_O}$$

It follows that v_O' is larger than v_O by the factor $1 + R_O/(R_L \| R_F)$. Because this is greater than unity, R_O causes the op amp to "work harder" to put out a larger output voltage. We conclude that a resistor should not be connected in series between the op amp output terminal and the connection for the feedback resistor.

1.2.2 The Inverting Amplifier with T Feedback Network

If a high voltage gain is required from an inverting amplifier, Eq. (1.3) shows that either R_F must be large, R_1 must be small, or both. If R_1 is small, the input resistance given by Eq. (1.4) may be too low to meet specifications. The inverting amplifier with a T feedback network shown in Fig. 1.5(a) can be used to obtain a high voltage gain without a small value for R_1 or very large values for the feedback resistors.

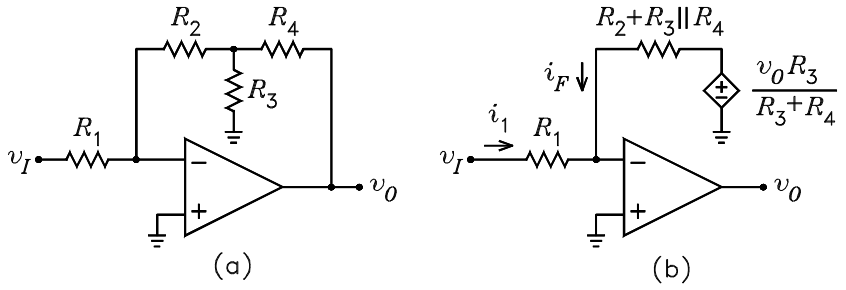

Figure 1.5: (a) Inverting amplifier with a T feedback network. (b) Equivalent circuit for calculating v_O.

The solution for the voltage gain is simplified by making a Thévenin equivalent circuit at the v_- terminal looking to the right through R_2. The circuit is given in Fig. 1.5(b). Because $i_1 + i_F = 0$, it follows that

$$\frac{v_I}{R_1} + \frac{v_O R_3}{R_3 + R_4} \times \frac{1}{R_2 + R_3 \| R_4} = 0 \tag{1.6}$$

This equation can be solved for the voltage gain to obtain

$$\frac{v_O}{v_I} = -\left[\frac{R_2}{R_1} + \frac{R_4}{R_1}\left(1 + \frac{R_2}{R_3}\right)\right] \tag{1.7}$$

The output resistance of the circuit is zero. The input resistance is R_1.

Example 4 *For the inverting amplifier with a T feedback network in Fig. 1.5(a), specify the resistor values which give an input resistance of* $10\,\text{k}\Omega$ *and a gain of* -100*. The maximum resistor value in the circuit is limited to* $100\,\text{k}\Omega$*.*

Solution. To meet the input resistance specification, we have $R_1 = 10\,\text{k}\Omega$. Let $R_2 = R_4 = 100\,\text{k}\Omega$. It follows from Eq. (1.7) that R_3 is given by

$$R_3 = \frac{R_2 R_4}{(-v_O/v_I)\,R_1 - (R_2 + R_4)}$$

This equation gives $R_3 = 12.5\,\text{k}\Omega$.

1.2.3 The Current-to-Voltage Converter

The circuit diagram of a *current-to-voltage* converter is shown in Fig. 1.6(a). The circuit is a special case of an inverting amplifier where the input resistor is replaced with a short circuit. Because the v_- terminal is a virtual ground, the input resistance is zero. The output resistance is also zero. Because $i_1 + i_F = 0$ and $v_O = i_F R_F$, it follows that the transresistance gain is given by

$$\frac{v_O}{i_1} = -R_F \tag{1.8}$$

Figure 1.6(b) shows the current-to-voltage converter with a current source connected to its input. Because R_S connects from a virtual ground to ground, the current through R_S is zero. It follows that $i_1 = i_S$ and $v_O = -R_F i_S$. Thus the output voltage is independent of R_S.

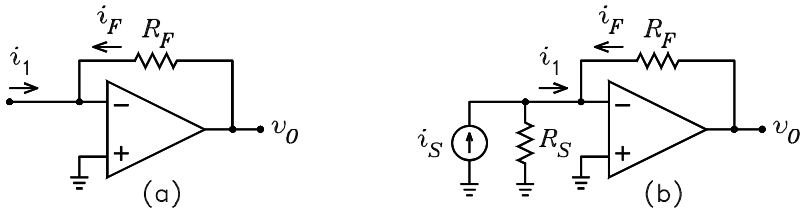

Figure 1.6: (a) Current-to-voltage converter. (b) Curcuit with an input current source.

1.3 Non-Inverting Amplifiers

1.3.1 The Non-Inverting Amplifier

Figure 1.7(a) shows the circuit diagram of a non-inverting amplifier. The input voltage v_I is applied to the non-inverting op amp input. A voltage divider consisting of resistors R_F and R_1 connects from the output node to the inverting input. The circuit is called a non-inverting amplifier because its voltage gain is positive. This means that if the input voltage is increasing or going positive, the output voltage will also be increasing or going positive. If the circuit diagrams of the inverting and the non-inverting amplifiers are compared, it can be seen that the circuits are the same if $v_I = 0$. Thus the only difference between the two circuits is the node at which the input voltage is applied.

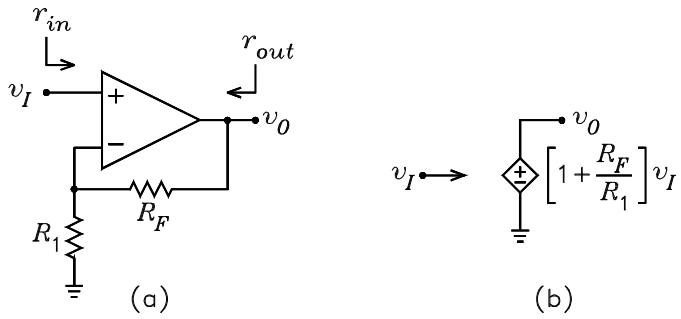

Figure 1.7: (a) Non-inverting amplifier. (b) Controlled-source model.

For the circuit of Fig. 1.7(a), the voltage difference between the two op amp input terminals is given by $v_+ - v_- = v_O/A$. For v_O finite and $A \to \infty$, it follows that $v_+ \to v_-$. It is said that a virtual short circuit exists between the two inputs because there is no voltage difference between the two terminals. For $i_- = 0$, the condition that $v_+ = v_-$ requires v_I and v_O to satisfy the equation

$$v_+ = v_- \qquad \Longrightarrow \qquad v_I = v_O \frac{R_1}{R_F + R_1} \tag{1.9}$$

where voltage division has been used for v_-. This can be solved for the voltage gain to obtain

$$\frac{v_O}{v_I} = 1 + \frac{R_F}{R_1} \tag{1.10}$$

The input and output resistances are given by

$$r_{in} = \infty \tag{1.11}$$

$$r_{out} = 0 \tag{1.12}$$

The controlled source model for the non-inverting amplifier is shown in Fig. 1.7(b).

Example 5 *Design a non-inverting amplifier which has an input resistance of* $10\,\text{k}\Omega$*, an open-circuit voltage gain of* 20 *(a decibel voltage gain of* $26\,\text{dB}$*), and an output resistance of* $600\,\Omega$*. The feedback network is specified to draw no more than* $0.1\,\text{mA}$ *from the output of the op amp when the open-circuit output voltage is in the range* $-10\,\text{V} \le v_O \le 10\,\text{V}$*.*

Solution. The circuit diagram for the amplifier is shown in Fig. 1.8. To meet the input resistance specification, we have $R_i = 10\,\text{k}\Omega$. For the specified current in the feedback network, we must have $0.1\,\text{mA} \le 10/(R_F + R_1)$. If the equality is used, we obtain $R_F + R_1 = 100\,\text{k}\Omega$. For the specified open-circuit voltage gain, Eq. (1.10) gives $1 + R_F/R_1 = 20$ or $R_F = 19R_1$. It follows that $R_1 = 5\,\text{k}\Omega$ and $R_F = 95\,\text{k}\Omega$. To meet the output resistance specification, we must have $R_O = 600\,\Omega$.

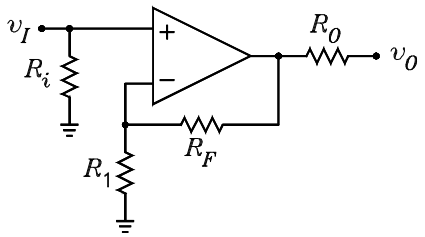

Figure 1.8: Circuit for Example 5.

Example 6 *Examine the effect of a connecting a resistor between the* v_+ *node and the* v_- *node in the non-inverting amplifier of the circuit for Example 5.*

Solution. For an ideal op amp, the voltage difference between the v_+ and v_- terminals is zero. It follows that a resistor connected between these nodes has no current flowing through it. Therefore, the resistor has no apparent effect on the circuit. This conclusion applies also for the inverting amplifier circuit of Fig. 1.3. With physical op amps, however, a resistor connected between the v_+ and the v_- terminals can affect the performance of the circuit by reducing the effective open-loop gain A.

1.3.2 The Voltage Follower

The voltage follower or unity-gain buffer is a unity-gain non-inverting amplifier. The circuit diagram is shown in Fig. 1.9(a). Compared to the non-inverting amplifier of Fig. 1.7(a), the feedback resistor R_F is replaced by a short circuit and resistor R_1 is omitted. Because the output node is connected directly to the inverting input instead of through a voltage divider, the circuit is said to have 100% feedback. Because $v_+ = v_-$, it follows that $v_O = v_I$. Therefore, the circuit has unity voltage gain. The voltage follower is often used to isolate a low resistance load from a high output resistance source. That is, the voltage follower supplies the current to drive the load while drawing no current from the input circuit.

Example 7 *Figure 1.9(b) shows a source connected to a load with a voltage follower. It is given that* $R_S = 10\,\text{k}\Omega$ *and* $R_L = 100\,\Omega$*. (a) Calculate* v_O*. (b) Calculate* v_O *if the voltage follower is removed and the source connected to the load.*

Solution. (a) With the voltage follower, there is no current through R_S so that the voltage at the op amp input is v_S. It follows that $v_O = v_S$. (b) If the voltage follower is removed and the source is connected directly to the load, v_O is given by $v_O = v_S R_L/(R_S + R_L) = v_S/101$. This is a decrease in output of $20 \log 101 = 40.1\,\text{dB}$. This example illustrates how a unity gain amplifier can increase the gain of a circuit.

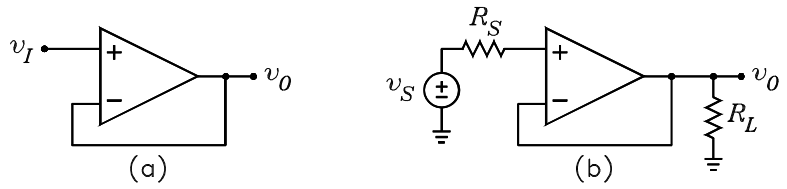

Figure 1.9: (a) Voltage follower. (b) Circuit for Example 7.

1.3.3 Amplifier with Voltage and Current Feedback

Figure 1.10(a) shows the circuit diagram of a non-inverting amplifier in which the voltage fed back to the inverting input of the op amp is a function of both the load voltage and the load current. To solve for the output voltage, it is convenient to first form the Thévenin equivalent circuit seen by the load resistor R_L. The circuit is shown in Fig. 1.10(b). It consists of a voltage source in series with a resistor. The voltage source has a value equal to the open-circuit load voltage, i.e. the output voltage with $R_L \to \infty$. The resistor has a value equal to the ratio of the open-circuit load voltage to the short-circuit load current, i.e. the output current with $R_L = 0$.

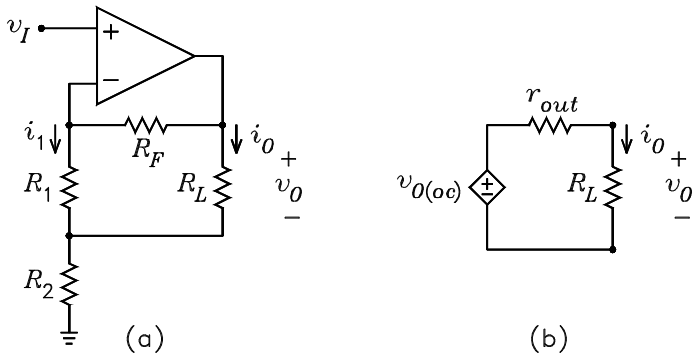

Figure 1.10: (a) Non-inverting amplifier with voltage and current feedback. (b) Thévenin equivalent circuit seen by the load.

With $R_L = \infty$, the open-circuit load voltage is given by $v_{O(oc)} = i_1 (R_F + R_1)$. Because there is a virtual short circuit between the v_+ and the v_- terminals, it follows that $i_1 = v_I / (R_1 + R_2)$. It follows that $v_{O(oc)}$ can be written

$$v_{O(oc)} = v_I \frac{R_1 + R_F}{R_1 + R_2} \tag{1.13}$$

With $R_L = 0$, there can be no current through R_F or R_1 so that $v_I = v_- = i_{O(sc)} R_2$. Thus $i_{O(sc)}$ is given by

$$i_{O(sc)} = \frac{v_I}{R_2} \tag{1.14}$$

The output resistance of the circuit is given by

$$r_{out} = \frac{v_{O(oc)}}{i_{O(sc)}} = R_2 \frac{R_1 + R_F}{R_1 + R_2} \tag{1.15}$$

By voltage division, it follows from Fig. 1.10(b) and Eq. (1.13) that the output voltage can be written

$$v_O = v_{O(oc)} \times \frac{R_L}{r_{out} + R_L} = v_I \frac{R_1 + R_F}{R_1 + R_2} \times \frac{R_L}{r_{out} + R_L} \tag{1.16}$$

1.3.4 The Negative Impedance Converter

Although it is not an amplifier, the negative impedance converter is an application of the non-inverting configuration. For the circuit in Fig. 1.11(a), the resistor R bridges the input and output terminals of a non-inverting amplifier. We can write

$$r_{in} = \frac{v_I}{i_1} \tag{1.17}$$

$$i_1 = \frac{v_I - v_O}{R} \tag{1.18}$$

$$v_O = \left(1 + \frac{R_F}{R_1}\right) v_I \tag{1.19}$$

Solution for r_{in} yields

$$r_{in} = -\frac{R_1}{R_F} R \tag{1.20}$$

Thus the circuit has a negative input resistance.

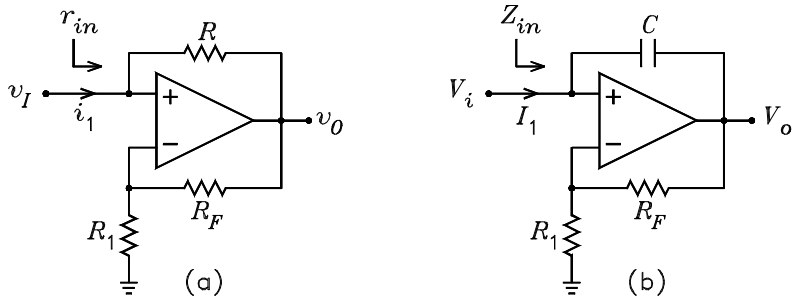

Figure 1.11: Negative impedance converters. (a) Negative input resistance. (b) Negative input capacitance.

A resistor in parallel with another resistor equal to its negative is an open circuit. It follows that the output resistance of a non-ideal current source. i.e. one having a non-infinite output resistance, can be made infinite by adding a negative resistance in parallel with the current source. Negative resistors do not absorb power from a circuit. Instead, they supply power. For example, if a capacitor with an initial voltage on it is connected in parallel with a negative resistor, the voltage on the capacitor will increase with time. Relaxation oscillators are waveform generator circuits which use a negative resistance in parallel with a capacitor to generate ac waveforms.

The resistor is replaced with a capacitor in Fig. 1.11(b). In this case, the input impedance is

$$Z_{in} = -\frac{R_1}{R_F} \frac{1}{j\omega C} = j\omega \frac{R_1}{\omega^2 R_F C} = j\omega L_{eq} \tag{1.21}$$

It follows that the input impedance is that of a frequency dependent inductor given by

$$L_{eq} = \frac{R_1}{\omega^2 R_F C} \tag{1.22}$$

1.4 Summing Amplifiers

1.4.1 The Inverting Summer

The inverting summer is the basic op amp circuit that is used to sum two or more signal voltages, to sum a dc voltage with a signal voltage, etc. An inverting summer with four inputs is shown in Fig. 1.12(a). If all

inputs are grounded except the v_{Ij} input, where $j = 1$, 2, 3, or 4, Eq. (1.3) for the inverting amplifier can be used to write $v_O = -(R_F/R_j)\, v_{Ij}$. It follows by superposition that the total output voltage is given by

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} - \frac{R_F}{R_3}v_{I3} - \frac{R_F}{R_4}v_{I4} \tag{1.23}$$

The input resistance to the jth input is R_j. The output resistance of the circuit is zero.

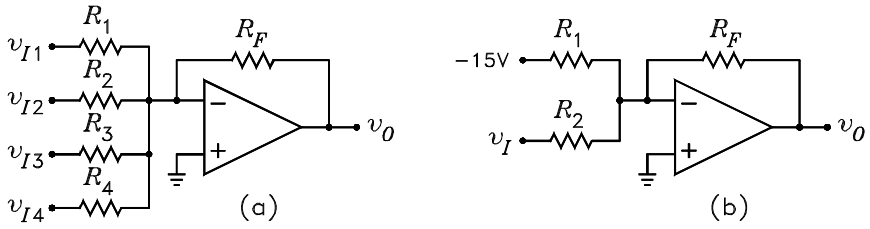

Figure 1.12: (a) Four input inverting summer. (b) Circuit for Example8.

Example 8 *Design an inverting summer which has an output voltage given by*

$$v_O = 3 - 2v_I$$

Assume that $+15\,\mathrm{V}$ *and* $-15\,\mathrm{V}$ *supply voltages are available.*

Solution. The output contains a dc term of $+3\,\mathrm{V}$. This can be realized by using the $-15\,\mathrm{V}$ supply as one input. The circuit is shown in Fig. 1.12(b). For the specified output, we can write $(-15)\times(-R_F/R_1) = 3$ and $-R_F/R_2 = -2$. If R_F is chosen to be $3\,\mathrm{k\Omega}$, it follows that $R_1 = 15\,\mathrm{k\Omega}$ and $R_2 = 1.5\,\mathrm{k\Omega}$.

1.4.2 The Non-Inverting Summer

A non-inverting summer can be realized by connecting the inputs through resistors to the input terminal of a non-inverting amplifier. Unlike the inverting amplifier, however, the input resistors do not connect to a virtual ground. Thus a current flows in each input resistor that is a function of the voltage at all inputs. This makes it impossible to define the input resistance for any one input unless all other inputs are grounded. The circuit diagram for a four-input non-inverting summer is shown in Fig. 1.13(a). To solve for the output voltage, it is convenient to first make Norton equivalent circuits at the v_+ terminal for each of the inputs. The circuit is shown in Fig. 1.13(b).

Eq. (1.10) can be used to write the equation for v_O as follows:

$$\begin{aligned} v_O &= v_+\left(1 + \frac{R_F}{R_6}\right) \\ &= \left(\frac{v_{I1}}{R_1} + \frac{v_{I2}}{R_2} + \frac{v_{I3}}{R_3} + \frac{v_{I4}}{R_4}\right)(R_1 \| R_2 \| R_3 \| R_4 \| R_5)\left(1 + \frac{R_F}{R_6}\right) \end{aligned} \tag{1.24}$$

The output resistance of the circuit is zero. If the v_{I2} through v_{I4} inputs are grounded, the input resistance to the v_{I1} node is given by

$$r_{in1} = R_1 + R_2 \| R_3 \| R_4 \| R_5 \tag{1.25}$$

The input resistance to the other inputs can be written similarly.

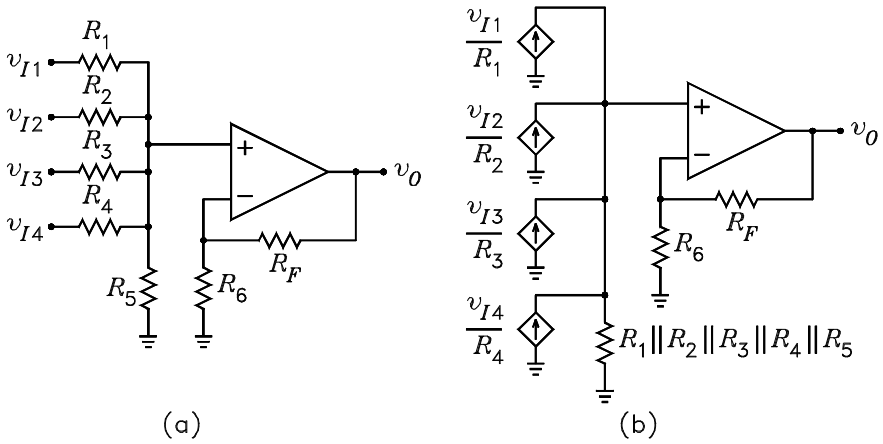

Figure 1.13: (a) Four input non-inverting summer. (b) Equivalent circuit for calculating v_O.

Example 9 *Design a two-input non-inverting summer which has an output voltage given by*

$$v_O = 8\,(v_{I1} + v_{I2})$$

With either input grounded, the input resistance to the other input terminal is specified to be $10\,\text{k}\Omega$*. In addition, the current which flows in the grounded input lead is to be* $1/10$ *the current that flows in the ungrounded lead.*

Solution. The circuit is shown in Fig. 1.14. By symmetry, it follows that $R_2 = R_1$. For the input resistance specification, we must have $R_1 + R_1 \| R_3 = 10\,\text{k}\Omega$. If v_{I2} is grounded, i_2 is given by current division $i_2 = -i_1 R_3/\,(R_3 + R_1)$. For $i_2 = -i_1/10$, we have $R_3/\,(R_3 + R_1) = 1/10$. It follows from these two equations that $R_3 = 10/9.9\,\text{k}\Omega = 1.01\,\text{k}\Omega$ and $R_1 = R_2 = 9R_3 = (10/1.1)\ \text{k}\Omega = 9.09\,\text{k}\Omega$.

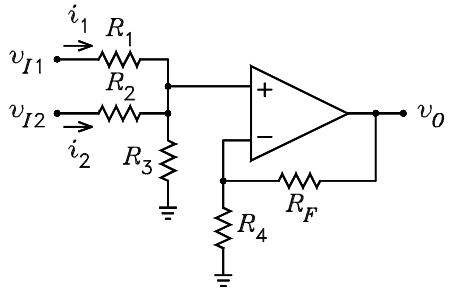

Figure 1.14: Circuit for Example 9.

If $v_{I1} = v_{I2} = v_I$, it follows that $v_O/v_I = 16$. Thus we can write the design equation

$$16 = \frac{v_+}{v_I} \times \frac{v_O}{v_+} = \frac{R_3}{R_3 + R_1/2}\left(1 + \frac{R_F}{R_4}\right)$$

It follows from this equation that $1 + R_F/R_4 = 88$. This can be achieved with $R_4 = 270\,\Omega$ and $R_F = 23.5\,\text{k}\Omega$.

1.5 Differential Amplifiers

1.5.1 The Single Op Amp Diff Amp

A *differential amplifier* or *diff amp* is an amplifier which has two inputs and one output. When a signal is applied to one input, the diff amp operates as a non-inverting amplifier. When a signal is applied to the other input, it acts as an inverting amplifier. The circuit diagram of a single op amp diff amp is shown in Fig. 1.15(a). Superposition can be used to write the equation for v_O as follows:

$$v_O = v_+ \left(1 + \frac{R_F}{R_3}\right) - v_{I2}\frac{R_F}{R_3} = v_{I1}\frac{R_2}{R_1 + R_2}\left(1 + \frac{R_F}{R_3}\right) - v_{I2}\frac{R_F}{R_3} \tag{1.26}$$

where Eqs. (1.3) and (1.10) have been used.

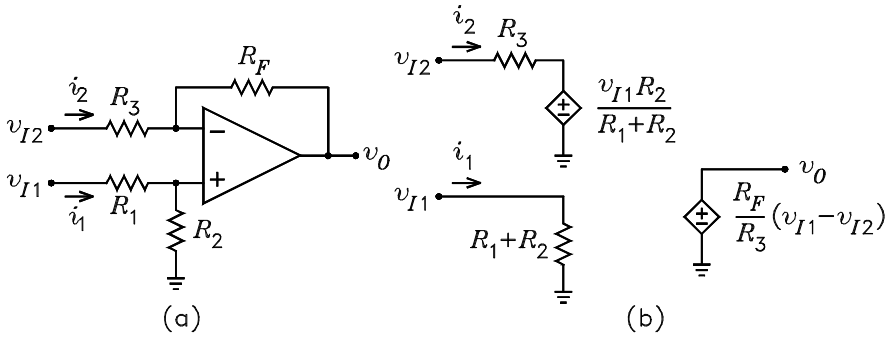

Figure 1.15: (a) Diff amp circuit. (b) Equivalent circuit for the special case of a true diff amp.

The output resistance of the diff amp is zero. The input resistance to the v_{I1} node is given by

$$r_{in1} = R_1 + R_2 \tag{1.27}$$

The current i_2 which flows in the v_{I2} input lead is a function of the voltage at the v_{I1} input. It is given by

$$i_2 = \frac{v_{I2} - v_-}{R_3} = \frac{1}{R_3}\left(v_{I2} - v_{I1}\frac{R_2}{R_1 + R_2}\right) \tag{1.28}$$

where $v_- = v_+$ has been used. The input resistance to the v_{I2} input is given by $r_{in2} = v_{I2}/i_2$. It can be seen that r_{in2} is a function of v_{I1}. For example, $v_{I1} = 0$ gives $r_{in2} = R_3$, $v_{I1} = -v_{I2}$ gives $r_{in2} = R_3\,(R_1 + R_2)\,/\,(R_1 + 2R_2)$, $v_{I1} = +v_{I2}$ gives $r_{in2} = R_3\,(1 + R_2/R_1)$, etc.

1.5.2 The True Diff Amp

The output voltage of a *true diff amp* is zero if $v_{I1} = v_{I2}$. It follows from Eq. (1.26) that the condition for a true diff amp is

$$\frac{R_2}{R_1} = \frac{R_F}{R_3} \tag{1.29}$$

To achieve this condition, it is common to make $R_1 = R_3$ and $R_2 = R_F$. In this case, the output voltage can be written

$$v_O = \frac{R_F}{R_3}\,(v_{I1} - v_{I2}) \tag{1.30}$$

The controlled-source equivalent circuit of the single op amp true diff amp is shown in Fig. 1.15(b).

Example 10 *For the diff amp circuit of Fig. 1.15(a), it is given that* $R_1 = R_3 = 10\,\text{k}\Omega$ *and* $R_2 = R_F = 20\,\text{k}\Omega$. *Solve for the output voltage, the input resistance to the* v_{I1} *terminal, and the input resistance to the* v_{I2} *terminal for the three cases:* $v_{I1} = 0$, $v_{I1} = -v_{I2}$, *and* $v_{I1} = +v_{I2}$.

Solution. Because $R_F/R_3 = R_2/R_1$, the output voltage is given by Eq. (1.30). It follows that $v_O = 2\,(v_{I1} - v_{I2})$. The input resistance to the v_{I1} node is $30\,\text{k}\Omega$. As described above, the input resistance to the v_{I2} terminal is a function of v_{I1}. For $v_{I1} = 0$, it is $10\,\text{k}\Omega$. For $v_{I1} = -v_{I2}$, it is $6\,\text{k}\Omega$. For $v_{I1} = +v_{I2}$, it is $40\,\text{k}\Omega$.

1.5.3 Differential and Common-Mode Voltage Gains

Figure 1.16 shows a single op amp diff amp circuit with three sources at its input. The two input voltages are given by

$$v_{I1} = v_{CM} + \frac{v_D}{2} \tag{1.31}$$

$$v_{I2} = v_{CM} - \frac{v_D}{2} \tag{1.32}$$

The voltage v_{CM} is called the *common-mode input voltage* because it appears equally at both inputs. The voltage v_D is called the *differential input voltage* because one-half of its value appears at each input with opposite polarities.

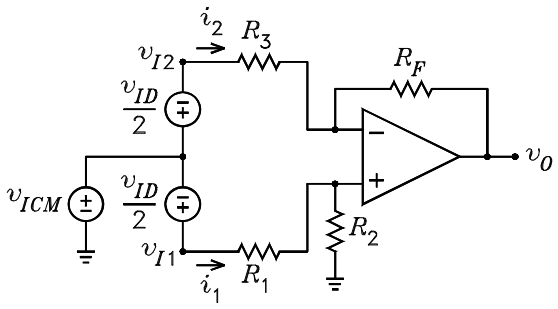

Figure 1.16: Diff amp with differential and common-mode input sources.

It is often convenient to analyze diff amp circuits by expressing the input voltages as common-mode and differential components. The voltages v_{CM} and v_D can be expressed in terms of v_{I1} and v_{I2} as follows:

$$v_D = v_{I1} - v_{I2} \tag{1.33}$$

$$v_{CM} = \frac{v_{I1} + v_{I2}}{2} \tag{1.34}$$

These two equations can be used to resolve any two arbitrary input voltages into differential and common-mode components. For example, $v_{I2} = 0$ gives $v_D = v_{I1}$ and $v_{CM} = v_{I1}/2$, $v_{I2} = -v_{I1}$ gives $v_D = 2v_{I1}$ and $v_{CM} = 0$, $v_{I2} = v_{I1}$ gives $v_D = 0$ and $v_{CM} = v_{I1}$, etc.

By Eq. (1.26), the output voltage of the diff amp in Fig. 1.16 can be written

$$\begin{aligned} v_O &= \left(v_{CM} + \frac{v_D}{2}\right)\frac{R_2}{R_1 + R_2}\left(1 + \frac{R_F}{R_3}\right) - \left(v_{CM} - \frac{v_D}{2}\right)\frac{R_F}{R_3}] \\ &= v_{CM}\frac{R_2}{R_1 + R_2}\left(1 - \frac{R_F R_1}{R_2 R_3}\right) + \frac{v_D}{2}\,\frac{R_F}{R_3}\left[1 + \frac{R_2\,(R_3 + R_F)}{R_F\,(R_1 + R_2)}\right] \end{aligned} \tag{1.35}$$

This equation can be used to define the differential and common-mode voltage gains, respectively, as follows:

$$A_d = \frac{v_O}{v_D} = \frac{R_F}{2R_3}\left[1 + \frac{R_2\,(R_3 + R_F)}{R_F\,(R_1 + R_2)}\right] \tag{1.36}$$

$$A_{cm} = \frac{v_O}{v_{CM}} = \frac{R_2}{R_1 + R_2}\left(1 - \frac{R_F R_1}{R_2 R_3}\right) \tag{1.37}$$

If $R_F/R_2 = R_3/R_1$, these equations give $A_d = R_F/R_3$ and $A_{cm} = 0$.

1.5.4 The Common-Mode Rejection Ratio

For a true diff amp, the common-mode voltage gain is zero. In practice, it is difficult to achieve a common-mode gain that is exactly zero because of resistor tolerances. A figure of merit for the true diff amp is the ratio of its differential voltage gain to its common-mode voltage gain. This is called the *common-mode rejection ratio* or $CMRR$. Ideally, it is infinite. The $CMRR$ of the circuit in Fig. 1.16 is given by

$$CMRR = \frac{A_d}{A_{cm}} = \frac{\frac{R_F}{2R_3}\left[1 + \frac{R_2(R_3+R_F)}{R_F(R_1+R_2)}\right]}{\frac{R_2}{R_1+R_2}\left[1 - \frac{R_F R_1}{R_2 R_3}\right]} \tag{1.38}$$

This is often expressed in decibels by the relation $20\log(CMRR)$.

Example 11 *For the diff amp in Fig. 1.17, solve for v_O, the current i, the resistance seen by the generator, v_{I1}, v_{I2}, and the common-mode input voltage.*

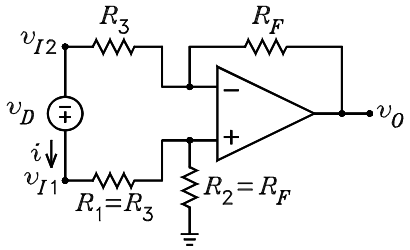

Figure 1.17: Circuit for Example 11.

Solution. By Eq. (1.30), v_O is given by

$$v_O = \frac{R_F}{R_3} v_D$$

Because there is a virtual short circuit between the inverting and the non-inverting op amp inputs, it follows that i is given by

$$i = \frac{v_D}{2R_3}$$

Thus the generator sees the resistance $2R_3$. To solve for v_{I1} and v_{I2}, we can write

$$v_{I1} = i\,(R_3 + R_F) = \frac{v_D}{2R_3}\,(R_3 + R_F) = \frac{v_D}{2}\left(\frac{R_F}{R_3} + 1\right)$$

$$v_{I2} = v_{I1} - v_D = \frac{v_D}{2}\left(\frac{R_F}{R_3} - 1\right)$$

The common-mode component of v_{I1} and v_{I2} is given by

$$v_{CM} = \frac{v_{I1} + v_{I2}}{2} = \frac{R_F}{R_3} \times \frac{v_D}{2} = \frac{v_0}{2}$$

Thus the op amp forces a common-mode voltage at the two diff amp inputs that is equal to one-half the output voltage.

1.5.5 The Switch Hitter

The single op amp diff amp circuit of Fig. 1.18(a) is known as a *switch hitter*. The signal applied to the non-inverting op amp input is taken from the wiper of a potentiometer. To solve for the output voltage as a function of the position of the wiper, we denote the potentiometer resistance from wiper to ground by xR_p, where $0 \leq x \leq 1$. By voltage division, it follows that the voltage at the non-inverting op amp input is $v_+ = xv_I$. The circuit is redrawn in Fig. 1.18(b) with separate sources driving the inverting and the non-inverting inputs. By superposition of the two sources, the output voltage can be written

$$v_O = 2v_+ - v_I = (2x - 1)\, v_I \tag{1.39}$$

where Eqs. (1.3) and (1.10) have been used. It follows that the voltage gain of the circuit is $2x - 1$. This has the values -1 for $x = 0$, 0 for $x = 0.5$, and $+1$ for $x = 1$. Thus the circuit gain can be varied from -1 through 0 to $+1$ as the position of the potentiometer wiper is varied.

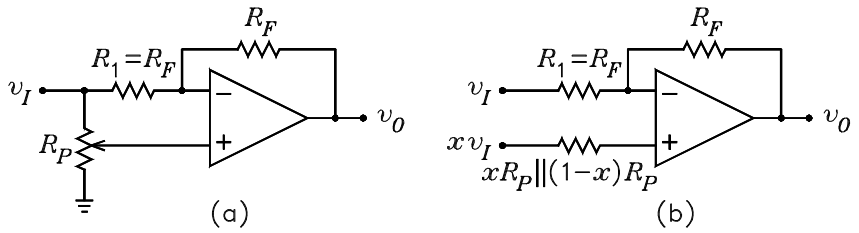

Figure 1.18: (a) Switch hitter. (b) Equivalent circuit.

1.5.6 The Two Op Amp Diff Amp

A two op amp diff amp is shown in Fig. 1.19. By superposition, the output voltage of this circuit is given by

$$v_O = -\frac{R_{F2}}{R_3} v_{01} - \frac{R_{F2}}{R_2} v_{I2} = \frac{R_{F1} R_{F2}}{R_1 R_3} v_{I1} - \frac{R_{F2}}{R_2} v_{I2} \tag{1.40}$$

where Eq. (1.3) has been used. The circuit operates as a true diff amp if either of two conditions is satisfied. These are $R_1 = R_{F1}$ and $R_3 = R_2$ or $R_1 = R_2$ and $R_{F1} = R_3$. Under either condition, the expression for the output voltage reduces to

$$v_O = \frac{R_{F2}}{R_2} (v_{I1} - v_{I2}) \tag{1.41}$$

The input resistance to the v_{I1} input is R_1. The input resistance to the v_{I2} input is R_2. The output resistance is zero.

The two op amp diff amp has two advantages over the single op amp diff amp. First, the input resistance to either input is not a function of the voltage at the other input. Thus the common-mode voltage at the inputs cannot be a function of the output voltage as it is with the single op amp diff amp. Second, when the circuit is used as a true diff amp, the differential voltage gain can be varied by varying a single resistor without simultaneously changing the common-mode voltage gain. This resistor is R_{F2}. The single op amp diff amp does not have this feature.

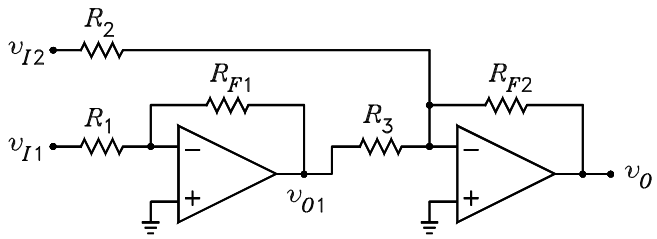

Figure 1.19: Two op amp diff amp.

Example 12 *Design a two op amp diff amp which has a differential voltage gain of* 20*, a common-mode voltage gain of 0, and an input resistance to each input of* $10\,\text{k}\Omega$*.*

Solution. For the circuit of Fig. 1.19, the input resistance specifications can be met with $R_1 = R_2 = 10\,\text{k}\Omega$. For the differential gain specification, it follows from Eq. (1.41) that $R_{F2}/R_2 = 20$. Thus we must have $R_{F2} = 200\,\text{k}\Omega$. For a common-mode gain of zero, we must have either $R_1 = R_{F1}$ and $R_3 = R_2$ or $R_1 = R_2$ and $R_{F1} = R_3$. Because we have already specified that $R_1 = R_2$, we must have $R_{F1} = R_3$. The value for these resistors is arbitrary. We specify $R_{F1} = R_3 = 200\,\text{k}\Omega$.

1.5.7 The Instrumentation Amplifier

The diff amp circuit of Fig. 1.20 is known as an *instrumentation amplifier*. In some applications, it is called an *active transformer*. To solve for v_O, we use superposition of the inputs v_{I1} and v_{I2}. With $v_{I2} = 0$, the v_- terminal of op amp 2 is at virtual ground and op amp 1 operates as a non-inverting amplifier. By Eq. (1.10), its output voltage is given by

$$v_{O1} = \left(1 + \frac{R_{F1}}{R_1}\right) v_{I1} \tag{1.42}$$

Because there is a virtual short circuit between the v_+ and v_- inputs of op amp 1, the voltage at the lower node of R_1 is v_{I1}. It follows that op amp 2 operates as an inverting amplifier. By Eq. (1.3), its output voltage is given by

$$v_{O2} = -\frac{R_{F1}}{R_1} v_{I1} \tag{1.43}$$

Op amp 3 operates as a true diff amp. By Eq. (1.30), its output voltage is given by

$$v_O = \frac{R_{F2}}{R_2}\left(v_{O1} - v_{O2}\right) = \frac{R_{F2}}{R_2}\left(1 + 2\frac{R_{F1}}{R_1}\right) v_{I1} \tag{1.44}$$

Similarly, for $v_{I1} = 0$, v_O is given by

$$v_O = -\frac{R_{F2}}{R_2}\left(1 + 2\frac{R_{F1}}{R_1}\right) v_{I2} \tag{1.45}$$

By superposition, the total output voltage is

$$v_O = \frac{R_{F2}}{R_2}\left(1 + 2\frac{R_{F1}}{R_1}\right)\left(v_{I1} - v_{I2}\right) \tag{1.46}$$

This is the voltage output of a true diff amp. The input resistance to each input of the amplifier is infinite. The output resistance is zero.

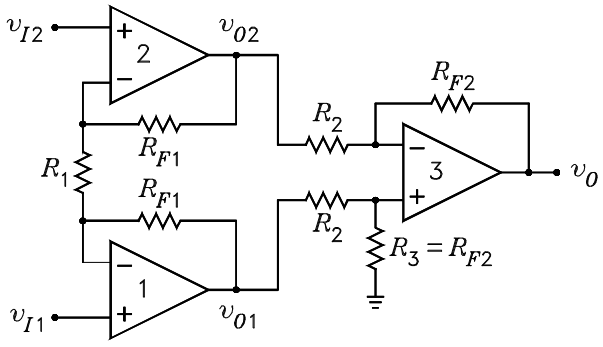

Figure 1.20: Instrumentation amplifier.

The instrumentation amplifier can be thought of as the cascade connection of two amplifiers. The first stage consists of op amps 1 and 2. Let its voltage gain be denoted by A_1. The second stage consists of op amp 3. Let its voltage gain be denoted by A_2. The two gains are given by

$$A_1 = \frac{v_{O1} - v_{O2}}{v_{I1} - v_{I2}} = 1 + 2\frac{R_{F1}}{R_1} \tag{1.47}$$

$$A_2 = \frac{v_O}{v_{O1} - v_{O2}} = \frac{R_{F2}}{R_2} \tag{1.48}$$

It can be seen that A_1 represents the ratio of a differential output voltage to a differential input voltage.

The instrumentation amplifier is used in applications where a true diff amp is required with a very high common-mode rejection ratio. A potentiometer connected as a variable resistor in series with R_1 can be used to adjust the voltage gain without simultaneously changing the common-mode rejection ratio. A potentiometer connected as a variable resistor in series with R_3 can be used to optimize the $CMRR$. To do this experimentally, the two inputs are connected together and a common-mode signal voltage applied. The potentiometer in series with R_3 is adjusted for minimum output voltage.

Example 13 *Design an instrumentation amplifier which has a differential voltage gain of* 100 *(a decibel gain of* 40 dB*) and a common-mode voltage gain of zero.*

Solution. The gain of 100 must be divided between the two stages of the circuit. It is convenient to give the input stage, consisting of op amps 1 and 2, a gain of 10 and the second stage, consisting of op amp 3, a gain of 10. Using Eqs. (1.47) and (1.48), we can write the two design equations

$$1 + 2\frac{R_{F1}}{R_1} = 10 \qquad \text{and} \qquad \frac{R_{F2}}{R_2} = 10$$

With two equations and four unknowns, it is necessary to assign values to two of the resistors. Let $R_{F1} = R_{F2} = 10\,\text{k}\Omega$. It follows that $R_2 = 1\,\text{k}\Omega$ and $R_1 = (10/4.5)\ \text{k}\Omega = 2.22\,\text{k}\Omega$.

1.5.8 The Differential Output Amplifier

Figure 1.21 shows the circuit diagram of a *differential output amplifier*. This circuit has two output voltages which have opposite polarities. That is, if v_{O1} is positive, v_{O2} will be negative, and vice versa. Because the lower node of resistor R_1 is at virtual ground, Eq. (1.10) can be used to write for v_{O1}

$$v_{O1} = \left(1 + \frac{R_{F1}}{R_1}\right) v_I \tag{1.49}$$

Because there is a virtual short between the inverting and non-inverting inputs to op amp 1, the upper node of R_1 sees the input voltage v_I. Thus Eq. (1.3) can be use to write for v_{O2}

$$v_{O2} = -\frac{R_{F2}}{R_1} v_I \tag{1.50}$$

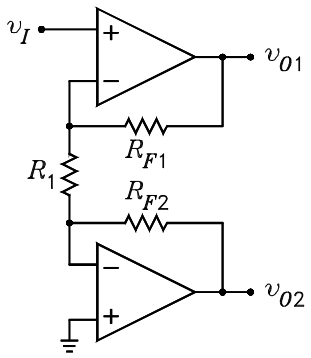

Figure 1.21: Differential output amplifier.

In most applications of the differential output amplifier, the condition $v_{O2} = -v_{O1}$ is desired. When this is satisfied, the amplifier is said to be a *balanced* differential output amplifier. This requires the condition $1 + R_{F1}/R_1 = R_{F2}/R_1$ which reduces to

$$R_{F1} = R_{F2} - R_1 \tag{1.51}$$

In this case, the output voltages can be written

$$v_{O1} = -v_{O2} = \frac{R_{F2}}{R_1} v_I \tag{1.52}$$

The differential output voltage is given by

$$v_{O1} - v_{O2} = \frac{2R_{F2}}{R_1} v_I \tag{1.53}$$

Example 14 *Design a balanced differential output amplifier with an open-circuit voltage gain of* 4*, an input resistance of* $10\,\text{k}\Omega$*, and a balanced output resistance of* $600\,\Omega$*. The amplifier is to drive a* $600\,\Omega$ *load. If the maximum peak output voltage from each op amp is* $\pm 12\,\text{V}$*, calculate the maximum peak load voltage and the output level in dBm for a sine wave input signal. (The dBm is the decibel output power referenced to the power* $P_{ref} = 1\,\text{mW}$*.)*

Solution. The circuit is shown in Fig. 1.22. For the input resistance specification, we have $R_i = 10\,\text{k}\Omega$. For an open-circuit voltage gain of 4, it follows from Eq. (1.53) that $2R_{F2}/R_1 = 4$. This can be satisfied by choosing $R_{F2} = 20\,\text{k}\Omega$ and $R_1 = 10\,\text{k}\Omega$. Eq. (1.51) gives $R_{F1} = 10\,\text{k}\Omega$. To achieve a $600\,\Omega$ balanced output resistance, we must have $R_{O1} = R_{O2}$ and $R_{O1} + R_{O2} = 600$. It follows that $R_{O1} = R_{O2} = 300\,\Omega$. If the voltage output of op amp 1 peaks at $+12\,\text{V}$, the voltage output from op amp 2 peaks at $-12\,\text{V}$ and the peak load voltage is $v_P = 24 \times 600/\,(600 + 600) = 12\,\text{V}$, where voltage division has been used. The output level in dBm is given by

$$\text{Output Level } = 10\log\left(\frac{v_P^2/2R_L}{P_{ref}}\right) = 10\log\left(\frac{12^2/1200}{0.001}\right) = 20.8\,\text{dBm}$$

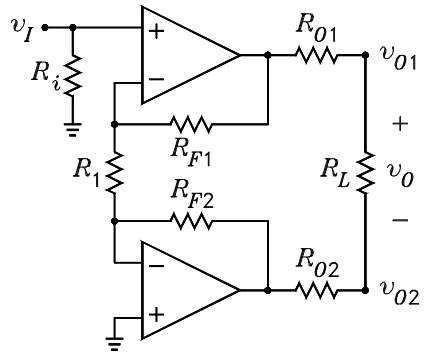

Figure 1.22: Circuit for Example 14.

1.6 Op Amp Differentiators

1.6.1 The Ideal Differentiator

A *differentiator* is a circuit which has an output voltage that is proportional to the time derivative of its input voltage. Fig. 1.23 gives the circuit diagram of an op amp differentiator. The circuit is similar to the inverting amplifier in Fig. 1.3 with the exception that resistor R_1 is replaced by a capacitor. It follows that Eq. (1.3) can be used to solve for the voltage gain transfer function of the differentiator by replacing R_1 with the complex impedance of the capacitor. The voltage gain transfer function is given by

$$\frac{V_o}{V_i} = -\frac{R_F}{(1/C_1 s)} = -R_F C_1 s \tag{1.54}$$

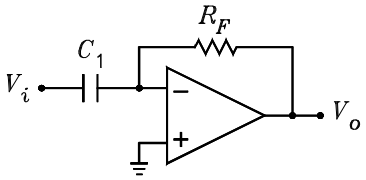

Figure 1.23: Ideal differentiator.

Because a multiplication by s in the complex frequency domain is equivalent to a differentiation in the time domain, it follows from the above equation that the time domain output voltage is given by

$$v_O(t) = -R_F C_1 \frac{dv_I(t)}{dt} \tag{1.55}$$

Thus the circuit has the transfer function of an inverting differentiator with the gain constant $R_F C_1$. Because the gain constant has the units of seconds, it is called the *differentiator time constant*. The output resistance of the circuit is zero. The input impedance transfer function is that of the capacitor C_1 to virtual ground given by

$$Z_{in} = \frac{1}{C_1 s} \tag{1.56}$$

With $s = j\omega$, it follows that $|Z_{in}| \to 0$ as ω becomes large. This is a disadvantage because a low input impedance can cause large currents to flow in the input circuit.

1.6.2 The Modified Differentiator

With $s = j\omega$, it follows from Eq. (1.54) that the magnitude of the voltage gain of the differentiator is $\omega R_F C_1$. For large ω, the gain can get very high. This is a disadvantage in circuits where out-of-band high-frequency noise can be a problem. To limit the high-frequency gain, a resistor can be used in series with C_1 as shown in Fig. 1.24(a). This also has the advantage that the high-frequency input impedance does not approach zero. At high frequencies where C_1 is a short, the gain magnitude is limited to the value R_F/R_1 and the input impedance approaches R_1. The voltage gain transfer function of the circuit with R_1 is given by

$$\frac{V_o}{V_i} = -\frac{R_F}{R_1 + 1/C_1 s} = -R_F C_1 s \times \frac{1}{1 + R_1 C_1 s} \tag{1.57}$$

This is of the form of the transfer function of a differentiator multiplied by the transfer function of a low-pass filter which has a pole time constant $R_1 C_1$.

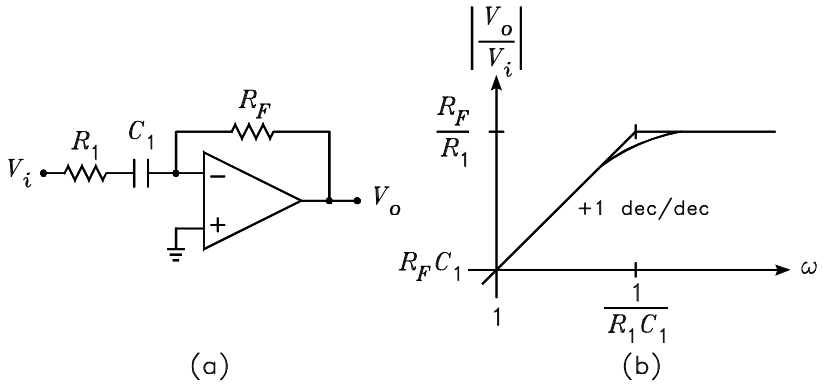

Figure 1.24: (a) Modified differentiator. (b) Bode plot for $|V_o/V_i|$.

The Bode magnitude plot for the transfer function of Eq. (1.57) is given in Fig. 1.24(b). For $\omega << 1/R_1C_1$, the asymptotic plot exhibits a slope of +1 dec/dec which is the proper slope for a differentiator. In this band, the voltage gain is given by $V_o/V_i \cong -j\omega R_F C_1$. At $\omega = 1$, the magnitude of the gain is $R_F C_1$. For $\omega >> 1/R_1C_1$, the asymptotic slope is 0 and the magnitude of the gain shelves at the value R_F/R_1. It follows that the circuit with R_1 acts as a differentiator only for frequencies such that $\omega << 1/R_1C_1$. The input impedance transfer function of the circuit with R_1 is given by

$$Z_{in} = R_1 + \frac{1}{C_1 s} = R_1 \times \frac{1 + R_1 C_1 s}{R_1 C_1 s} \tag{1.58}$$

This is of the form of a constant multiplied by the reciprocal of a high-pass transfer function. For $s = j\omega$, it follows that $|Z_{in}| \to R_1$ as ω becomes large.

Example 15 *Design a modified differentiator which has a time constant of* 10 ms *and a pole frequency of* 1 kHz. *For a* 1 V *peak sine-wave input signal at* 100 Hz, *calculate the peak sine wave output voltage and the relative phase of the output voltage.*

Solution. The circuit is shown in Fig. 1.24(a). For the gain constant specification, we must have $R_F C_1 = 0.01$. If we let $C_1 = 0.1\,\mu$F, it follows that $R_F = 100\,\text{k}\Omega$. For the pole frequency of 1000 Hz, we must have $R_1 C_1 = 1/2\pi 1000$. This gives $R_1 = 10,000/2\pi = 1.59\,\text{k}\Omega$. From Eq. (1.57), the voltage gain magnitude at $f = 100$ Hz is given by

$$\left|\frac{V_o}{V_i}\right| = \left|-\frac{R_F C_1\,(j2\pi 100)}{1 + j2\pi 100 R_1 C_1}\right| = \frac{0.01 \times 2\pi 100}{\sqrt{1 + 0.1^2}} = 6.25$$

For a 1 V peak input sine wave at 100 Hz, it follows that the peak output voltage is 6.25 V. It follows from Eq. (1.57) that the phase of the output signal with respect to the input signal is given by

$$\varphi = +90^o - \tan^{-1}(2\pi 100 R_1 C_1) = 84.3^\circ$$

A perfect differentiator would have a phase of $+90^\circ$. Thus there is a phase error of -5.7°. Note that the negative sign in Eq. (1.57) does not affect the phase. This is because a negative sign indicates an inversion whereas a phase shift is associated with a shift in time. If a sine wave is observed on the screen of an oscilloscope, an inversion would flip the sine wave about the time axis. A phase shift would shift the position of the zero crossings along the time axis.

1.7 The Integrator

1.7.1 The Ideal Inverting Integrator

An *integrator* is a circuit which has an output voltage that is proportional to the time integral of its input voltage. The circuit for the integrator can be obtained by interchanging the resistor and the capacitor in the differentiator of Fig. 1.23. The circuit is shown in Fig. 1.25. The voltage gain transfer function is obtained from Eq. (1.3) by replacing R_F with the complex impedance of the capacitor C_F to obtain

$$\frac{V_o}{V_i} = -\frac{(1/C_F s)}{R_1} = -\frac{1}{R_1 C_F s} \tag{1.59}$$

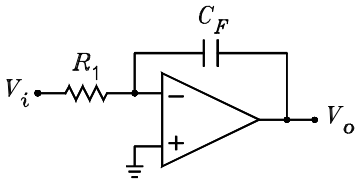

Figure 1.25: Inverting integrator.

Because a division by s in the complex frequency domain is equivalent to an integration in the time domain, it follows from this equation that the time domain output voltage is given by

$$v_O(t) = -\frac{1}{R_1 C_F}\int_{-\infty}^{t} v_I(\tau)\, d\tau \tag{1.60}$$

Thus the circuit has the transfer function of an inverting integrator with the gain constant $1/R_1 C_F$. Because $R_1 C_F$ has the units of seconds, it is called the *integrator time constant*. The input resistance to the circuit is R_1. The output resistance is zero.

1.7.2 The Modified Inverting Integrator

At zero frequency, C_F is an open circuit and the op amp in the integrator circuit loses feedback. For non-ideal op amps, this can cause undesirable dc offset voltages at the output. To provide feedback at dc, a resistor can be used in parallel with C_F as shown in Fig. 1.26(a). At low frequencies where C_F is an open circuit, the magnitude of the voltage gain is limited to the value R_F/R_1. The transfer function for the voltage gain of the integrator with R_F is given by

$$\frac{V_o}{V_i} = -\frac{R_F \| (1/C_F s)}{R_1} = -\frac{1}{R_1 C_F s} \times \frac{R_F C_F s}{1 + R_F C_F s} \tag{1.61}$$

where Eq. (1.3) has been used. This is of the form of the transfer function of an ideal integrator multiplied by the transfer function of a high-pass filter which has the pole time constant $R_F C_F$. The Bode magnitude plot for the transfer function is given in Fig. 1.26(b). For $\omega << 1/R_F C_F$, the plot exhibits a slope of 0. For $\omega >> 1/R_F C_F$, the slope is -1 dec/dec which is the proper slope for an integrator. It follows that the circuit with R_F acts as an integrator only for frequencies such that $\omega >> 1/R_F C_F$.

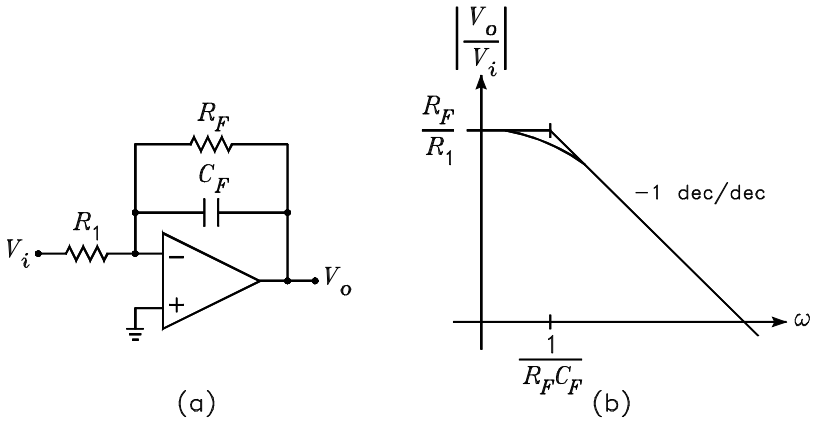

Figure 1.26: (a) Modified inverting integrator. (b) Bode magnitude plot for $|V_o/V_i|$.

Example 16 *Design a modified integrator which has a time constant of* 0.1 s *and a pole frequency of* 1 Hz. *For a* 1 V *peak sine-wave input signal at* 10 Hz, *calculate the peak sine-wave output voltage and the relative phase of the output voltage.*

Solution. The circuit is shown in Fig. 1.26(a). For the time constant specification, we have $R_1 C_F = 0.1$. If we take $C_F = 0.1\,\mu$F, it follows that $R_1 = 1\,$MΩ. For the pole frequency of 1 Hz, we must have $R_F C_F = 1/2\pi$. This gives $R_F = 1/\left(2\pi \times 0.1 \times 10^{-6}\right) = 1.59\,$MΩ. From Eq. (1.61), the gain magnitude at $f = 10\,$Hz is given by

$$\left|\frac{V_o}{V_i}\right| = \left|-\frac{1}{j2\pi 10 R_1 C_F} \times \frac{j2\pi 10 R_F C_F}{1 + j2\pi 10 R_F C_F}\right| = \frac{1.59}{\sqrt{1+10^2}} = 0.158$$

For a 1 V peak input sine wave at 100 Hz, it follows that the peak output voltage is 0.158 V.

It follows from Eq. (1.61) that the phase of the output signal with respect to the input signal is given by

$$\varphi = -\tan^{-1}\left(2\pi 10 R_F C_F\right) = -84.3\,^\circ$$

A perfect integrator would have a phase of $-90\,^\circ$. Thus there is a phase error of $+5.7\,^\circ$. As is discussed in Example 15, the negative sign in Eq. (1.61) indicates that the output signal is inverted with respect to the input signal and does not represent a phase shift.

1.7.3 The Non-Inverting Integrator

The circuit diagram of a *non-inverting integrator* is shown in Fig. 1.27(a). The voltage output from the op amp is fed back to both its inverting input and to its non-inverting input. Thus the circuit has both positive and negative feedback. To solve for the voltage gain transfer function, it is convenient to make two Norton equivalent circuits at the V_+ node, one looking toward the input through the left R and the other looking toward the output through the right R. The circuit obtained is shown in Fig. 1.27(b), where the two parallel

resistors are combined into a single resistor of value $R/2$. Because there is a virtual short between the V_+ and the V_- inputs, we can write

$$\frac{V_o}{2} = \left(\frac{V_i}{R} + \frac{V_o}{R}\right)\left(\frac{R}{2}\|\frac{1}{Cs}\right) = (V_i + V_o)\,\frac{1}{1 + RCs/2} \tag{1.62}$$

This equation can be solved for the voltage gain transfer function of the circuit to obtain

$$\frac{V_o}{V_i} = \frac{2}{RCs} \tag{1.63}$$

This is the transfer function of a non-inverting integrator with the gain constant $2/RC$. The time constant of the integrator is $RC/2$.

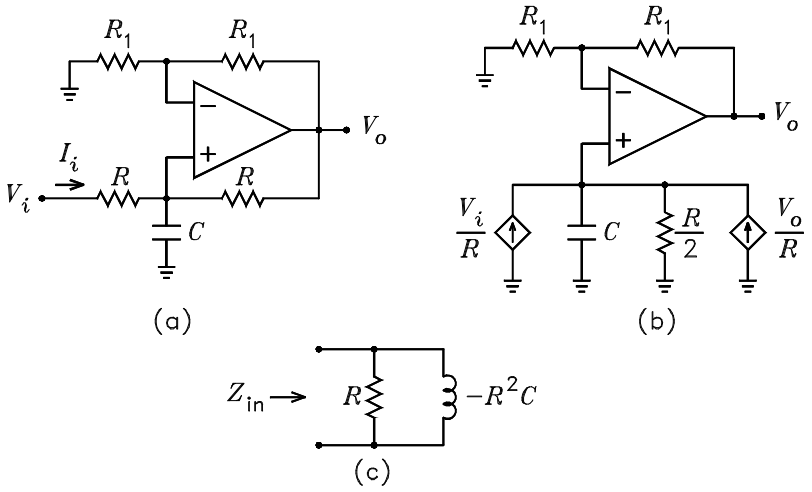

Figure 1.27: (a) Non-inverting integrator. (b) Equivalent circuit for calculating V_o. (c) Equivalent circuit for Z_{in}.

The input current in the circuit of Fig. 1.27(a) can be solved for as follows:

$$I_i = \frac{V_i - V_+}{R} = \frac{V_i - V_-}{R} = \frac{V_i}{R}\left(1 - \frac{1}{RCs}\right) \tag{1.64}$$

where $V_- = V_o/2$ has been used. This equation can be solved for the input impedance transfer function to obtain

$$Z_{in} = \frac{V_i}{I_i} = \frac{R\left(-R^2Cs\right)}{R + \left(-R^2Cs\right)} \tag{1.65}$$

The equivalent circuit which has this impedance is a resistor R in parallel with a negative inductor $-R^2C$. The equivalent circuit is given in Fig. 1.27(c). Because the inductor is a short circuit at zero frequency, it follows that the input impedance to the circuit is zero for a dc source.

Example 17 *The non-inverting integrator of Fig. 1.27(a) has the circuit element values* $R = 1\,\text{k}\Omega$ *and* $C = 1\,\mu\text{F}$. *For a sine wave input signal, calculate the voltage gain of the circuit at the frequency* $f = 100\,\text{Hz}$. *In addition, calculate numerical values for the circuit elements in the equivalent circuit for the input impedance.*

Solution. The voltage gain at $f = 100\,\text{Hz}$ is calculated from Eq. (1.63) as follows:

$$\frac{V_o}{V_i} = \frac{2}{10^3 \times 10^{-6}} \times j2\pi 100 = -j3.17$$

From Eq. (1.65), it follows that the input impedance circuit consists of a $1000\,\Omega$ resistor to ground in parallel with a negative inductor to ground having the value $-1000^2 \times 10^{-6} = -1\,\text{H}$.

1.8 Low-Pass Amplifiers

1.8.1 The Inverting Low-Pass Amplifier

This section covers several of the many op amp circuits which have a voltage gain transfer function that is of the form of single-pole low-pass and low-pass shelving transfer functions. Fig. 1.28(a) shows the circuit of an *inverting low-pass amplifier*. The voltage gain is obtained from Eq. (1.3) by replacing R_F with $R_F \| (1/C_F s)$. It is given by

$$\frac{V_o}{V_i} = -\frac{R_F \| (1/C_F s)}{R_1} = -\frac{R_F}{R_1} \times \frac{1}{1 + R_F C_F s} \tag{1.66}$$

This is of the form of a gain constant $-R_F/R_1$ multiplied by a low-pass transfer function having a pole time constant $R_F C_F$. The Bode magnitude plot for the transfer function is given in Fig. 1.28(b). The input resistance of the circuit is R_1. The output resistance is zero.

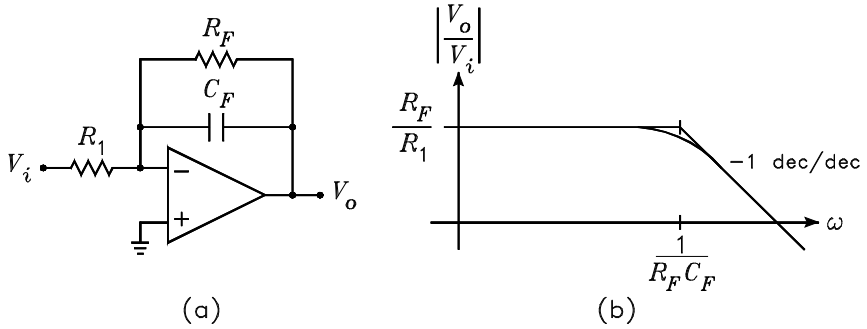

Figure 1.28: (a) Inverting low-pass amplifier. (b) Bode magnitude plot for $|V_o/V_i|$.

Example 18 *Design an inverting low-pass amplifier circuit which has an input resistance of* $10\,\text{k}\Omega$*, a low-frequency voltage gain of* -10*, and a pole frequency of* $10\,\text{kHz}$*.*

Solution. The circuit diagram of the amplifier is shown in Fig. 1.28(a). For an input resistance of $10\,\text{k}\Omega$, we have $R_1 = 10\,\text{k}\Omega$. The voltage gain transfer function is given by Eq. (1.66). For a low-frequency gain of -10, we have $R_F = 10R_1 = 100\,\text{k}\Omega$. For a pole frequency of $10\,\text{kHz}$, we have $C_F = 1/2\pi 10^4 R_F = 159\,\text{pF}$.

A second inverting low-pass amplifier circuit is shown in Fig. 1.29(a). The currents I_1, I_2, and I_F are given by

$$I_1 = \frac{V_i}{R_1 + (1/Cs) \| R_2} \tag{1.67}$$

$$I_2 = I_1 \frac{1/Cs}{R_2 + 1/Cs} = I_1 \frac{1}{1 + R_2 Cs} \tag{1.68}$$

$$I_F = \frac{V_o}{R_F} \tag{1.69}$$

where it is assumed that the V_- op amp input is at virtual ground and current division has been used for I_2. The voltage gain of the circuit can be obtained from the relation $I_2 + I_F = 0$ to obtain

$$\frac{V_o}{V_i} = -\frac{R_F}{R_1 + R_2} \times \frac{1}{1 + R_1 \| R_2 Cs} \tag{1.70}$$

This is of the form of a gain constant $-R_F/(R_1+R_2)$ multiplied by a low-pass transfer function having a pole time constant $(R_1\|R_2)\,C$. The Bode magnitude plot for the transfer function is given in Fig. 1.29(b).

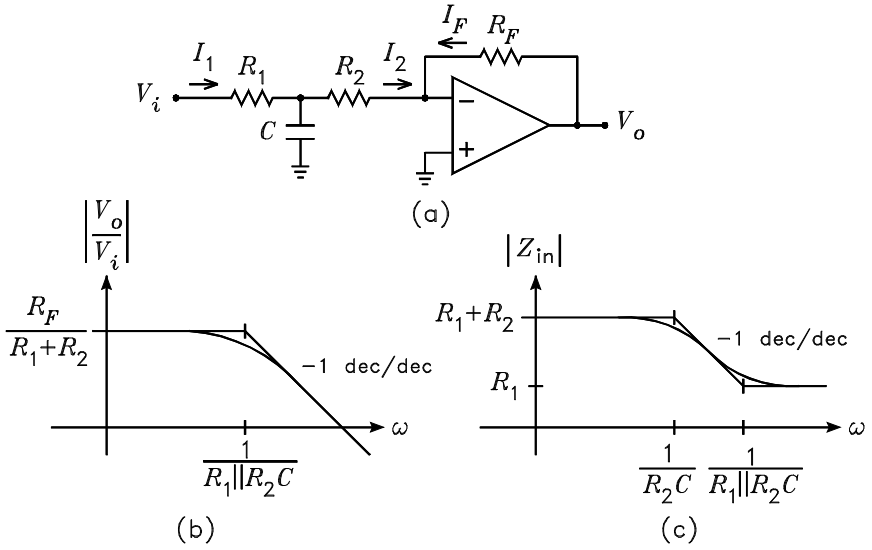

Figure 1.29: (a) Inverting low-pass amplifier. (b) Bode magnitude plot for $|V_o/V_i|$. (c) Bode magnitude plot for $|Z_{\rm in}|$.

The output resistance of the circuit is zero. The input impedance is given by

$$Z_{in} = R_1 + \frac{1}{Cs}\|R_2 = (R_1+R_2)\,\frac{1+(R_1\|R_2)\,Cs}{1+R_2Cs} \tag{1.71}$$

This transfer function is in the form of a low-pass shelving function having a pole time constant R_2C and a zero time constant $(R_1\|R_2)\,C$. The Bode magnitude plot of the impedance is given in Fig. 1.29(c). The low-frequency impedance is R_1+R_2. As frequency is increased, the impedance decreases and shelves at the value R_1.

Example 19 *Specify the circuit element values for the circuit of Fig. 1.29(a) for an inverting voltage gain of unity and a pole time constant of* $75\,\mu$s. *What is the pole frequency in the voltage-gain transfer function?*

Solution. Let $C = 0.01\,\mu$F and $R_2 = R_1$. It follows from Eq. (1.31) that $(R_1\|R_2)\,C = (R_1/2)\,C = 75\times10^{-6}$. Solution for R_1 and R_2 yields $R_1 = R_2 = 15\,\text{k}\Omega$. For an inverting voltage gain of unity, we must have $R_F = R_1+R_2 = 30\,\text{k}\Omega$. The pole frequency in the transfer function has the frequency $f = 1/\left(2\pi75\times10^{-6}\right) = 2.12\,\text{kHz}$.

1.8.2 The Non-Inverting Low-Pass Amplifier

Figure 1.30(a) shows a *non-inverting low-pass amplifier* consisting of a non-inverting amplifier with a RC low-pass filter at its input. The voltage gain transfer function of the circuit is given by

$$\frac{V_o}{V_i} = \frac{V_+}{V_i}\times\frac{V_o}{V_+} = \frac{1/Cs}{R+1/Cs}\left(1+\frac{R_F}{R_1}\right) = \left(1+\frac{R_F}{R_1}\right)\times\frac{1}{1+RCs} \tag{1.72}$$

where voltage division and Eq. (1.10) have been used. This is of the form of a gain constant $1+R_F/R_1$ multiplied by the transfer function of a low-pass filter having a pole time constant RC. The Bode magnitude

plot for the transfer function is given in Fig. 1.30(b). The output resistance of the circuit is zero. The input impedance is given by

$$Z_{in} = R + \frac{1}{Cs} = R \times \frac{1 + RCs}{RCs} \tag{1.73}$$

This is of the form of a resistor R multiplied by the reciprocal of a high-pass transfer function.

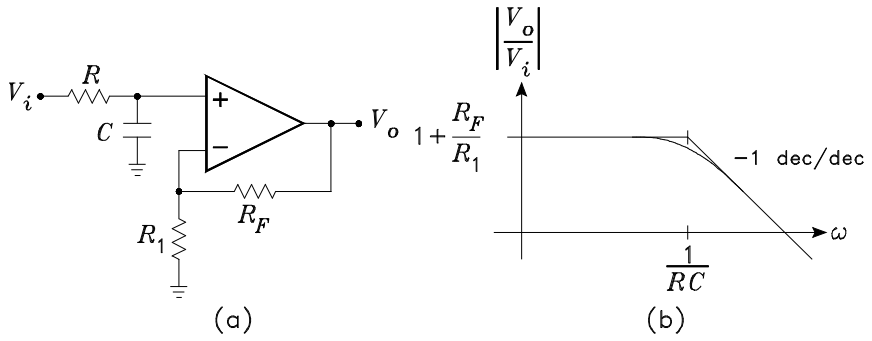

Figure 1.30: (a) Non-inverting low-pass amplifier. (b) Bode magnitude plot for $|V_o/V_i|$.

Example 20 *The non-inverting amplifier of Fig. 1.30(a) is to be designed for a voltage gain of* 12. *The input low-pass filter is to have a cutoff frequency of* 100 kHz. *Specify the element values for the circuit.*

Solution. To meet the cutoff frequency specification, it follows from Eq. (1.72) that $RC = 1/\left(2\pi 10^5\right)$. Either a value for R or a value for C must be specified before the other can be calculated. Let $C = 510\,\text{pF}$. It follows that $R = 3.12\,\text{k}\Omega$. For a gain of 12, we must have $1 + R_F/R_1 = 12$. If we choose $R_1 = 1\,\text{k}\Omega$, it follows that $R_F = 11\,\text{k}\Omega$.

1.8.3 The Non-Inverting Low-Pass Shelving Amplifier

The circuit diagram of a *non-inverting low-pass shelving amplifier* is shown in Fig. 1.31(a). The voltage gain is obtained from Eq. (1.8) by replacing R_F with $R_F \| \left(1/C_F s\right)$. It is given by

$$\frac{V_o}{V_i} = 1 + \frac{R_F \| \left(1/C_F s\right)}{R_1} = \left(1 + \frac{R_F}{R_1}\right) \frac{1 + R_F \| R_1 C_F s}{1 + R_F C_F s} \tag{1.74}$$

This is of the form of a gain constant $1 + R_F/R_1$ multiplied by a low-pass shelving transfer function having a pole time constant $R_F C_F$ and a zero time constant $\left(R_F \| R_1\right) C_F$. The Bode magnitude plot for the voltage gain is shown in Fig. 1.31(b). The low-frequency gain is $1 + R_F/R_1$. As frequency is increased, the gain decreases and shelves at unity.

Example 21 *The circuit of Fig. 1.31(a) is to be designed for a low-frequency gain of* 2 *(a* 6 dB *boost). The zero frequency in the transfer function is to be* 100 Hz. *Specify the circuit element values and calculate the frequency at which the voltage gain is* 3 dB.

Solution. For a low-frequency gain of 2, it follows from Eq. (1.74) that $1 + R_F/R_1 = 2$, which gives $R_F = R_1$. For the zero in the transfer function to be at 100 Hz, it follows that $R_F \| R_1 C_F = 1/\left(2\pi 100\right)$. If we choose $C_F = 0.1\,\mu\text{F}$, it follows that $R_1 = R_F = 31.8\,\text{k}\Omega$. With $s = j2\pi f$, the voltage gain transfer function can be written

$$\frac{V_o}{V_i} = 2\frac{1 + jf/100}{1 + jf/50}$$

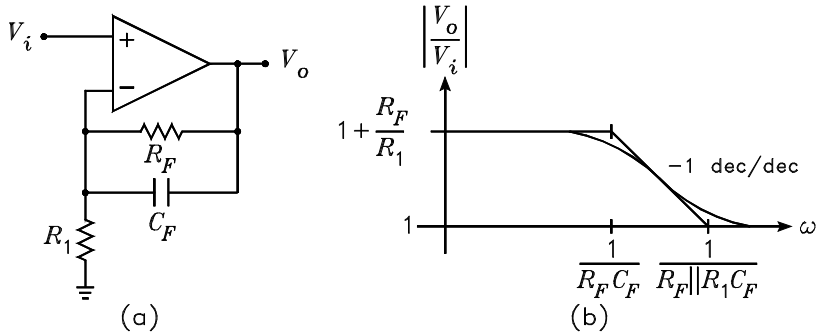

Figure 1.31: (a) Non-inverting low-pass shelving amplifier. (b) Bode magnitude plot for $|V_o/V_i|$.

At the 3 dB boost frequency, we have $|V_o/V_i|^2 = 1/2$. This condition gives

$$\frac{1+(f/100)^2}{1+(f/50)^2} = \frac{1}{2}$$

This can be solved for f to obtain $f = 100/\sqrt{2} = 70.7\,\text{Hz}$.

1.9 High-Pass Amplifiers

1.9.1 The Inverting High-Pass Amplifier

This section covers several of the many op amp circuits which have a voltage gain that is of the form of high-pass and high-pass shelving transfer functions. Fig. 1.32(a) shows an *inverting high-pass amplifier* circuit. The voltage gain is obtained from Eq. (1.3) by replacing R_1 with $R_1 + 1/(C_1 s)$. It is given by

$$\frac{V_o}{V_i} = -\frac{R_F}{R_1 + 1/(C_1 s)} = -\frac{R_F}{R_1} \times \frac{R_1 C_1 s}{1 + R_1 C_1 s} \tag{1.75}$$

This is of the form of a gain constant $-R_F/R_1$ multiplied by a high-pass transfer function having a pole time constant $R_1 C_1$. The Bode magnitude plot for the voltage gain is given in Fig. 1.32(b). The output resistance of the circuit is zero. The input impedance transfer function is given by

$$Z_{in} = R_1 + \frac{1}{C_1 s} = R_1 \times \frac{1 + R_1 C_1 s}{R_1 C_1 s} \tag{1.76}$$

This is of the form of a resistance R_1 multiplied by the reciprocal of a high-pass transfer function.

Example 22 *Design an inverting high-pass amplifier circuit which has a gain of* -10 *and a pole time constant of* $500\,\mu\text{s}$. *The input impedance to the circuit is to be* $10\,\text{k}\Omega$ *or higher. Calculate the lower half-power cutoff frequency of the amplifier.*

Solution. The circuit is shown in Fig. 1.32(a). The voltage-gain transfer function is given by Eq. (1.75). For the gain specification, we must have $R_F/R_1 = 10$. For the pole time constant specification, we must have $R_1 C_1 = 500 \times 10^{-6}$. Because there are three unknowns and only two equations, one of the circuit elements must be specified before the others can be calculated. Eq. (1.76) shows that the lowest value of the input impedance is R_1. Thus we must have $R_1 \geq 10\,\text{k}\Omega$. If $R_1 \geq 10\,\text{k}\Omega$, it follows that $C_1 \leq 0.05\,\mu\text{F}$. Let us choose $C_1 = 0.033\,\mu\text{F}$. It follows that $R_1 = 15.2\,\text{k}\Omega$ and $R_2 = 152\,\text{k}\Omega$. The lower half-power cutoff frequency is $f = 1/\left(2\pi \times 500 \times 10^{-6}\right) = 318\,\text{Hz}$.

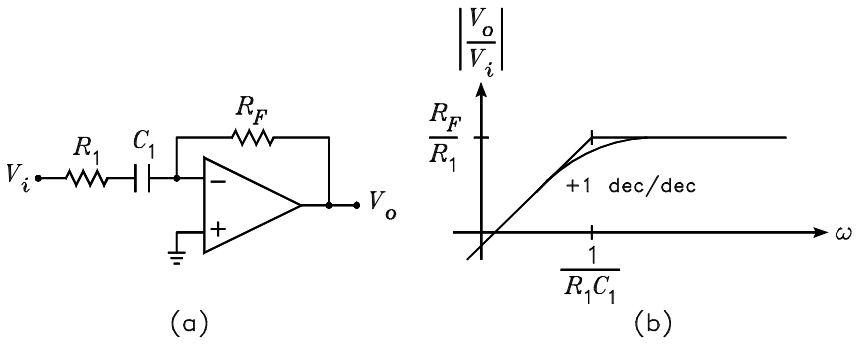

Figure 1.32: (a) Inverting high-pass amplifier. (b) Bode magnitude plot for $|V_o/V_i|$.

1.9.2 The Non-Inverting High-Pass Amplifier

Figure 1.33(a) shows a *non-inverting high-pass amplifier* circuit. The voltage gain transfer function is given by

$$\frac{V_o}{V_i} = \frac{V_+}{V_i} \times \frac{V_o}{V_+} = \frac{R}{R + 1/(Cs)} \left(1 + \frac{R_F}{R_1}\right) = \left(1 + \frac{R_F}{R_1}\right) \times \frac{RCs}{1 + RCs} \tag{1.77}$$

where voltage division and Eq. (1.10) have been used. This is of the form of a gain constant $(1 + R_F/R_1)$ multiplied by a single-pole high-pass transfer function having a pole time constant RC. The Bode magnitude plot for the voltage gain is given in Fig. 1.33(b). The output resistance of the circuit is zero. The input impedance transfer function is given by

$$Z_{in} = R + \frac{1}{Cs} = R \times \frac{1 + RCs}{RCs} \tag{1.78}$$

This is of the form of a resistance R multiplied by the reciprocal of a high-pass transfer function.

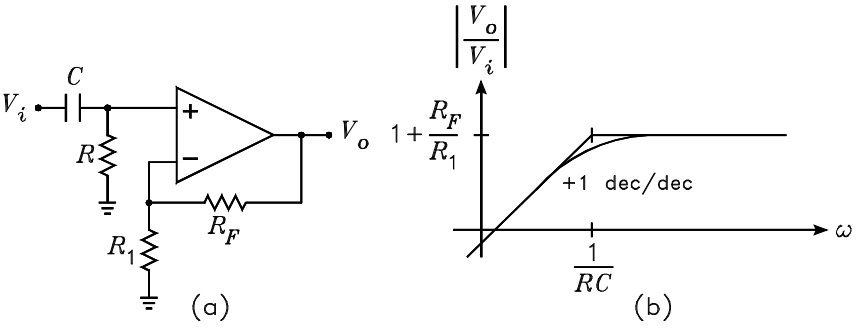

Figure 1.33: (a) Non-inverting high-pass amplifier. (b) Bode magnitude plot for $|V_o/V_i|$.

Example 23 *Design a non-inverting high-pass amplifier which has a gain of* 15 *and a lower cutoff frequency of* 20 Hz. *The input resistance to the amplifier is to be* 10 kΩ *in its passband.*

Solution. The circuit is shown in Fig. 1.33(a). In the amplifier passband, C is a short circuit. To meet the input resistance specification, we must have $R = 10\,\text{k}\Omega$. The voltage-gain transfer function is given by Eq. (1.77). For a lower half-power cutoff frequency of 20 Hz, we must have $RC = 1/(2\pi 20)$. Solution for C yields $C = 0.796\ \mu\text{F}$. For the gain specification, we must have $1 + R_F/R_1 = 15$ or $R_1 = R_F/14$. If $R_F = 56\,\text{k}\Omega$, it follows that $R_1 = 4\,\text{k}\Omega$.

1.9.3 The Non-Inverting High-Pass Shelving Amplifier

The circuit diagram of a *non-inverting high-pass shelving amplifier* is shown in Fig. 1.34(a). The voltage gain is given by Eq. (1.10) with R_1 replaced by $R_1 + 1/(C_1 s)$. It follows that the gain can be written

$$\frac{V_o}{V_i} = 1 + \frac{R_F}{R_1 + (1/C_1 s)} = \frac{1 + (R_F + R_1) C_1 s}{1 + R_1 C_1 s} \tag{1.79}$$

This is of the form of a high-pass shelving transfer function having a pole time constant $R_1 C_1$ and a zero time constant $(R_F + R_1) C_1$. The Bode magnitude plot for the voltage gain is shown in Fig. 1.34(b). It can be seen from the figure that the gain at low frequencies is unity. At high frequencies, the gain shelves at $1 + R_F/R_1$.

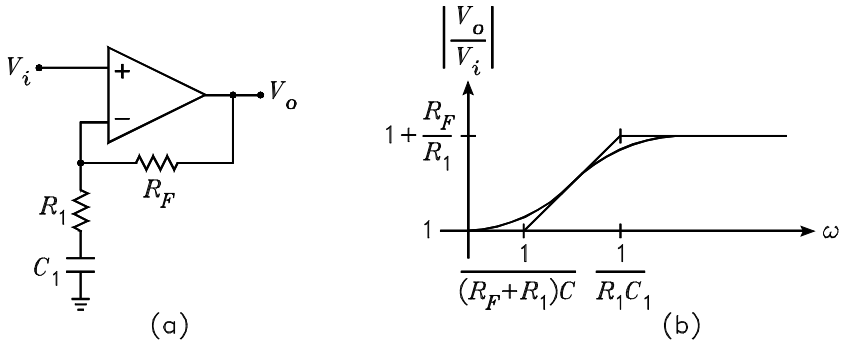

Figure 1.34: (a) Non-inverting high-pass shelving amplifier. (b) Bode magnitude plot for $|V_o/V_i|$.

Example 24 *Design a high-pass shelving amplifier which has unity gain at low frequencies, a pole in its transfer function with a time constant of* $75\,\mu$s*, and a zero with a time constant of* $7.5\,\mu$s*. What are the pole and zero frequencies and what is the gain at high frequencies?*

Solution. The circuit is shown in Fig. 1.34(a). The voltage-gain transfer function is given by Eq. (1.79). For the pole time constant specification, we must have $R_1 C_1 = 7.5\,\mu$s. For the zero time constant specification, we must have $(R_1 + R_F) C_1 = 75\,\mu$s. Because there are three circuit elements and only two equations, we must specify one element in order to calculate the other two. Let $C_1 = 0.001\,\mu$F. It follows that $R_1 = 7.5\,\text{k}\Omega$ and $R_2 = 75\,\text{k}\Omega - R_1 = 67.5\,\text{k}\Omega$. The zero frequency is $f_z = 1/\left(2\pi \times 75 \times 10^{-6}\right) = 2.12\,\text{kHz}$. The pole frequency is $f_p = 1/\left(2\pi \times 7.5 \times 10^{-6}\right) = 21.2\,\text{kHz}$. The gain at high frequencies is $1 + R_F/R_1 = 1 + 67.5/7.5 = 10$.

1.10 The Op Amp as a Comparator

1.10.1 The Inverting Comparator

A *comparator* is an active circuit element which has two input terminals and one output terminal. The output voltage exhibits two stable states. The output state depends on the relative value of one input voltage compared to the other input voltage. The op amp is often used as a comparator. Fig. 1.35(a) shows the circuit diagram of an op amp used as an *inverting comparator*. The voltage applied to the non-inverting input is the dc reference voltage V_{REF}. The output voltage is given by

$$v_O = A\,(V_{REF} - v_I) \tag{1.80}$$

where A is the voltage gain of the op amp. For an ideal op amp, we assume that $A \to \infty$. This implies that $v_O \to \infty$ for $v_I < V_{REF}$ and $v_O \to -\infty$ for $v_I > V_{REF}$. However, a physical op amp cannot have an infinite output voltage. Let us denote the maximum value of the magnitude of the output voltage by V_{SAT}. We call V_{SAT} the *saturation voltage* of the op amp.

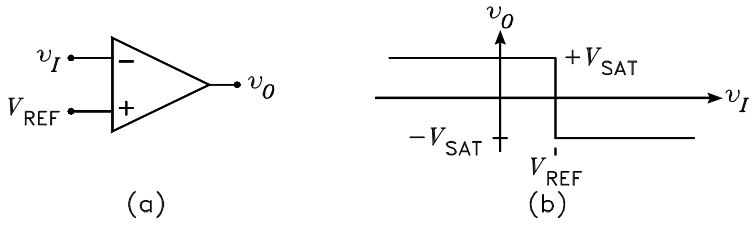

Figure 1.35: (a) Inverting comparator. (b) Plot of v_O versus v_I.

For an ideal op amp that exhibits saturation of its output voltage, the output voltage of the inverting comparator circuit in Fig. 1.35(a) can be written

$$v_O = V_{SAT}\,\mathrm{sgn}\,(V_{REF} - v_I) \tag{1.81}$$

where $\mathrm{sgn}(x)$ is the *signum* or *sign function* defined by $\mathrm{sgn}\,(x) = +1$ for $x > 0$ and $\mathrm{sgn}\,(x) = -1$ for $x < 0$. The plot of v_O versus v_I for the circuit is given in Fig. 1.35(b).

1.10.2 The Non-Inverting Comparator

Fig. 1.36(a) shows the circuit diagram of an op amp used as a *non-inverting comparator*. The output voltage of the circuit is given by

$$v_O = V_{SAT}\,\mathrm{sgn}\,(v_I - V_{REF}) \tag{1.82}$$

The graph of v_O versus v_I is given in Fig. 1.36(b).

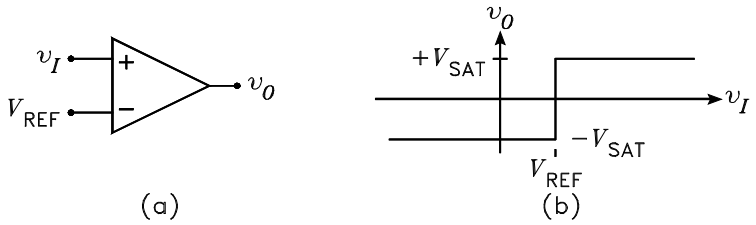

Figure 1.36: (a) Non-inverting comparator. (b) Plot of v_O versus v_I.

1.10.3 The Comparator with Positive Feedback or Schmitt Trigger

Positive feedback is often used with comparator circuits. The feedback is applied from the output to the non-inverting input of the op amp. This is in contrast to the circuits covered in the preceding sections of this chapter where feedback is applied to the inverting input. (The non-inverting integrator is an exception. This circuit uses feedback to both op amp inputs.) Fig. 1.37(a) gives the circuit diagram of an inverting op amp comparator with positive feedback. The circuit is also called a *Schmitt trigger*. It is named after Otto H. Schmitt who was a graduate student when he invented it in 1934. The capacitor C_F in the figure is assumed to be an open circuit in the following. This capacitor is often used to improve the switching speed

of a comparator by increasing the amount of positive feedback at high frequencies. It has no effect on the input voltage at which the op amp switches states.

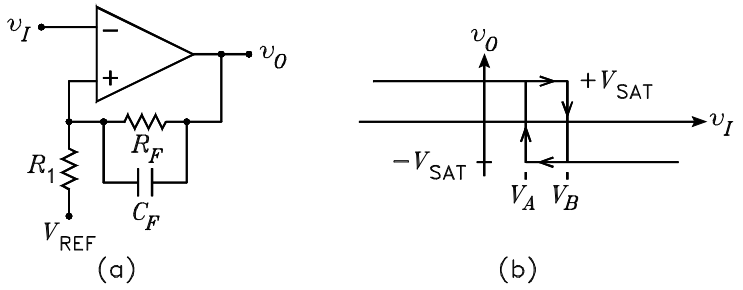

Figure 1.37: (a) Inverting comparator with positive feedback. (b) Plot of v_O versus v_I.

The output voltage from the circuit of Fig. 1.37(a) can be written

$$v_O = V_{SAT}\,\mathrm{sgn}\,(v_+ - v_I) \tag{1.83}$$

Because v_O has the two stable states $v_O = +V_{SAT}$ and $v_O = -V_{SAT}$, it follows that v_+ can have two stable states given by

$$V_A = V_{REF}\frac{R_F}{R_F + R_1} - V_{SAT}\frac{R_1}{R_F + R_1} \tag{1.84}$$

$$V_B = V_{REF}\frac{R_F}{R_F + R_1} + V_{SAT}\frac{R_1}{R_F + R_1} \tag{1.85}$$

where superposition and voltage division have been used for each equation. For $v_I < V_A$, it follows that $v_O = +V_{SAT}$. For $v_I > V_B$, it follows that $v_O = -V_{SAT}$. For $V_A < v_I < V_B$, v_O can have two stable states, i.e. $v_O = \pm V_{SAT}$. The graph of v_O versus v_I is given in Fig. 1.37(b).

The value of v_O for $V_A < v_I < V_B$ depends on whether v_I increases from a value less than V_A or v_I decreases from a value greater than V_B. That is, the circuit has memory. If $v_I < V_A$ initially and v_I begins to increase, v_O remains at the $+V_{SAT}$ state until v_I becomes greater than V_B. At this point v_O switches to the $-V_{SAT}$ state. If $v_I > V_B$ initially and v_I begins to decrease, v_O remains at the $-V_{SAT}$ state until v_I becomes less than V_A. Then v_O switches to the $+V_{SAT}$ state. The path for v_O on the graph in Fig. 1.37(b) is indicated with arrows. The loop in the graph is commonly called a *hysteresis loop.*

Example 25 *The Schmidt trigger circuit of Fig. 1.37(a) has the element values* $R_F = 1\,\mathrm{M}\Omega$ *and* $R_1 = 33\,\mathrm{k}\Omega$. *If* $V_{REF} = 3\,\mathrm{V}$ *and the op amp saturation voltage is* $V_{SAT} = 12\,\mathrm{V}$, *calculate the two threshold voltages* V_A *and* V_B.

Solution. By Eqs. (1.84) and (1.85), we have

$$V_A = 3\frac{1}{1 + 0.033} - 12\frac{0.033}{1 + 0.033} = 2.52\,\mathrm{V}$$

$$V_B = 3\frac{1}{1 + 0.033} + 12\frac{0.033}{1 + 0.033} = 3.29\,\mathrm{V}$$